MAX5857

16-Bit, 5.9Gsps Wideband Interpolating and Modulating RF DAC with JESD204B Interface

General Description

The MAX5857 high-performance, interpolating and modulating, 16-bit, 5.9Gsps RF DAC can directly synthesize up to 1.2GHz of instantaneous bandwidth from DC to frequencies greater than 2.6GHz. The device is optimized for cable access and digital video broadcast applications and meets spectral emission requirements for a broad set of radio transmitters and modulators including DOCSIS 3.1/3.0, DVB-C2, DVB-T2, DVB-S2X, ISDB-T, and EPoC.

The device integrates interpolation filters, a digital quadrature modulator, a numerically controlled oscillator (NCO), clock multiplying PLL+VCO and a 14-bit RF DAC core. The 4x linear phase interpolation filter simplifies reconstruction filtering, while enhancing passband dynamic performance and reducing the input data bandwidth required from an FPGA. The NCO allows for fully agile modulation of the input baseband signal for direct RF synthesis. The complex data path can be bypassed to access the RF DAC core directly.

The MAX5857 input interface accepts 16-bit input data through a six-lane JESD204B SerDes data input interface that is Subclass-0. The interface can be configured for 3, 4, 5, or 6 lanes and supports data rates up to 9.8304Gbps to optimize the I/O lane count and speed.

The MAX5857 clock input has a flexible interface that accepts a differential sine-wave or square-wave input clock signal up to 5.9GHz. A bypassable clock multiplying PLL and VCO can be used to internally generate the high-frequency sampling clock using a reference frequency between 245.76MHz and 1.475GHz. The device provides a divided reference clock to ensure synchronization between the data source and the DAC.

The integrated RF DAC uses a differential current-steering architecture that includes a differential 50Ω internal termination and can produce a 3.2dBm full-scale output signal level on a 50Ω external load. Operating from 1.0V and 1.8V power supplies, the device consumes 2.7W at 4.9Gsps. The device is offered in a compact 144-pin, 10mm x 10mm, FCCSP package and is specified for the extended industrial temperature range (-40°C to +85°C).

Ordering Information ***appears at end of data sheet.***

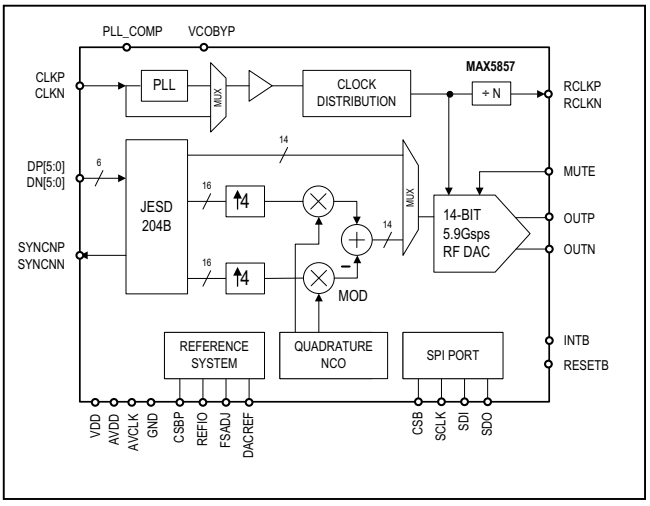
Benefits and Features

- Simplifies RF Design and Enables New Communication Architectures
  - Eliminates I/Q Imbalance and LO Feedthrough
  - Enables Multi-Band RF Modulation
- Direct RF Synthesis of 1.2GHz Bandwidth
  - 5.898Gsps DAC Output Update Rate
  - High-Performance 14-Bit RF DAC Core
  - Digital Baseband I/Q with 4x Interpolation
  - Bypass Path Without Interpolation for Real RF
  - Digital Quadrature Modulator+NCO for Full Agility
  - Sub-1Hz NCO Resolution
  - Integrated Clock Multiplying PLL+VCO
- Highly Flexible and Configurable
  - 3, 4, 5, or 6-Lane JESD204B Input Data Interface
  - Subclass-0 Compliant
  - Up to 9.8304Gbps Per Lane
  - Divided Reference Clock Output
  - SPI Interface for Device Configuration

Applications

- DOCSIS 3.1 Remote PHY and CCAP
- Digital Video Broadcast Modulators
  - DVB-C2/DVB-T2/DVB-S2X/ISDB-T
- Ethernet PON Over Coax (EPoC)
- Point-to-Point Wireless
- Instrumentation

Simplified Block Diagram



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Absolute Maximum Ratings

VDD2, AVCLK2, AVDD2, AVDD2PLL, VDD2PLL ....-0.3V to +2.1V
OUTP, OUTN .....-0.3V to (V_{AVDD2}+0.5)V
MUTE, RESETB, CSB, SCLK, SDO, SDI,
INTB, TDA ..... -0.3V to (V_{VDD2}+0.3, MAX 2.1)V
TESTP, TESTN, SYNCNP, SYNCNN,
RCLKP, RCLKN ..... -0.3V to (V_{VDD2} + 0.3, MAX 2.1)V
DP0, DN0, DP1, DN1, DP2, DN2, DP3, DN3,
DP4, DN4, DP5, DN5..... -0.3V to (V_{VDD2} + 0.3, MAX 1.6)V
JRES, CAPT, TESTEN ..... (V_{VSSPLL}-0.3)V to ($V_{VDD2PLL}$ + 0.3, MAX 2.1)V
VCOBYP.....-0.3V to (V_{AVCLK2} + 0.3, MAX 2.1)V
PLLCOMP .....-0.3V to ($V_{AVDD2PLL}$ + 0.3, MAX 2.1)V
VSSPLL, TDC, DACREF.....(V_{GND} – 0.3)V to (V_{GND} + 0.3)V
VDD, AVDD, AVCLK, AVDDPLL.....-0.3V to 1.2V
REFIO, FSADJ, CSBP..... -0.3V to (V_{AVDD2} + 0.3, MAX 2.1)V
CLKP, CLKN.....-0.3V to ($V_{AVDDPLL}$ + 0.3, MAX 1.2)V
SDO, INTB Maximum Continuous Current 8mA
Continuous Power Dissipation (T_A = +85°C).....4.0W
Thermal Characteristics:
Operating Temperature Range (T_A) ..... -40°C to +85°C
Operating Junction Temperature (T_J)..... +110°C
Maximum Junction Temperature .....+150°C
Storage Temperature Range ..... -60°C to +150°C
Soldering Temperature (reflow) .....+260°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Information

144 FCCSP

PACKAGE CODE	X14400F+1
Outline Number	21-0732
Land Pattern Number	90-0289
Thermal Resistance, Four-Layer Board:	
Junction to Ambient (θ_{JA})	16.2°C/W
Junction to Case (θ_{JC})	2.5°C/W

For the latest package outline information and land patterns (footprints), go to www.maximintegrated.com/packages. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to www.maximintegrated.com/thermal-tutorial.

Electrical Characteristics

(V_{DD} = V_{AVCLK} = V_{AVDD} = $V_{AVDDPLL}$ = 1.0V, V_{DD2} = V_{AVCLK2} = V_{AVDD2} = $V_{AVDD2PLL}$ = V_{DD2PLL} = 1.8V, P_{CLK} = 0dBm, f_{CLK} = 983.04MHz, f_{DAC} = 4915.2Msps, 4x interpolation, 5-lanes, 9830.4Mbps per lane, external reference at 1.206V, R_{SET} = 965Ω between FSADJ and DACREF, I_{OUTFS} = 40mA, output is 50Ω double-terminated and transformer coupled (see Figure 26), PLL ON. T_A ≥ -40°C and T_J ≤ +110°C (Note 1), unless otherwise noted. Typical values are at T_J = +65 ±15°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
STATIC PERFORMANCE						
Input Data Word Width	N			16		Bits
DAC Resolution				14		Bits
Differential Non-Linearity	DNL	Figure 27		±1.5		LSB
Integral Non-Linearity	INL	Figure 27		±3		LSB
Offset Voltage Error	OS			0.003		%FS
Minimum Full-Scale Output Current	I_{OUTFS}			10		mA

Electrical Characteristics (continued)

(V_{DD} = V_{AVCLK} = V_{AVDD} = $V_{AVDDPLL}$ = 1.0V, V_{DD2} = V_{AVCLK2} = V_{AVDD2} = $V_{AVDD2PLL}$ = V_{DD2PLL} = 1.8V, P_{CLK} = 0dBm, f_{CLK} = 983.04MHz, f_{DAC} = 4915.2Msps, 4x interpolation, 5-lanes, 9830.4Mbps per lane, external reference at 1.206V, R_{SET} = 965Ω between FSADJ and DACREF, I_{OUTFS} = 40mA, output is 50Ω double-terminated and transformer coupled (see Figure 26), PLL ON. T_A ≥ -40°C and T_J ≤ +110°C (Note 1), unless otherwise noted. Typical values are at T_J = +65 ±15°C.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Maximum Full-Scale Output Current	I_{OUTFS}				40		mA
Output-Voltage Gain Error	GE_{FS}	f_{OUT} = DC (Figure 27)			±3		%FS
Maximum Output Compliance					V_{AVDD2} + 0.4		V
Minimum Output Compliance					V_{AVDD2} - 0.4		V
Output Resistance	R_{OUT}	Differential DAC output resistance			50		Ω
DYNAMIC PERFORMANCE							
DAC Sample Rate	f_{DAC}					5898.24	Msps
Adjusted DAC Update Rate	AUR_{DAC}	(Note 2)				2949.12	Msps
Maximum Input Sample Rate	f_{S_IN}	For the complex I/Q dataset			1474.56		MHz
SFDR to Nyquist	SFDR	CW tone, -1dBFS	f_{OUT} = 500MHz		73		dB
			f_{OUT} = 1000MHz		74		
			f_{OUT} = 1500MHz		69		
Maximum HD2, HD3, $f_{DAC}/2-f_{OUT}$, Measured in 1st Nyquist Zone		CW tone, -3dBFS	f_{OUT} = 1842.5MHz		-71		dBc
Intermodulation Distortion	IMD	Two-tone signal, f_{DAC} = 5.898Gsps, f_1 = 1842MHz and f_2 = 1843MHz	Average total power -15dBFS		-74		dBc
			Average total power -33dBFS		-80		
Out-of-Band Noise and Spurious, Eight 6MHz 256-QAM Carriers	ACPR	f_{OUT} = 575MHz (Note 3)	Adjacent channel (Note 4) (Note 5)		-69.8	-62.9	dBc
			Next-adjacent channel (Note 4) (Note 5)		-70.5	-63.1	
			Third-adjacent channel (Note 4) (Note 5)		-70.9	-64.0	
			Noise in any other channel		-65.4		
		f_{OUT} = 975MHz, Average Total Power = -12dBFS (Note 6)	Adjacent channel (Note 5)		-67.4		
			Next-adjacent channel (Note 5)		-67.9		
			Third-adjacent channel (Note 5)		-68.5		
			Noise in any other channel		-63.8		

Electrical Characteristics (continued)

(V_{DD} = V_{AVCLK} = V_{AVDD} = $V_{AVDDPLL}$ = 1.0V, V_{DD2} = V_{AVCLK2} = V_{AVDD2} = $V_{AVDD2PLL}$ = V_{DD2PLL} = 1.8V, P_{CLK} = 0dBm, f_{CLK} = 983.04MHz, f_{DAC} = 4915.2Msps, 4x interpolation, 5-lanes, 9830.4Mbps per lane, external reference at 1.206V, R_{SET} = 965Ω between FSADJ and DACREF, I_{OUTFS} = 40mA, output is 50Ω double-terminated and transformer coupled (see Figure 26), PLL ON. T_A ≥ -40°C and T_J ≤ +110°C (Note 1), unless otherwise noted. Typical values are at T_J = +65 ±15°C.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Out-of-Band Noise and Spurious, Thirty-Two 6MHz 256-QAM Carriers	ACPR	f_{OUT} = 1100MHz, Average Total Power = -15dBFS (Note 6)	Adjacent channel (Note 5)		-64.4		dBc
			Next-adjacent channel (Note 5)		-64.1		
			Third-adjacent channel (Note 5)		-64.1		
			Noise in any other channel		-57.3		
Harmonic Distortion, Four 6MHz 256-QAM Carriers	HD	f_{OUT} = 575MHz, Average Total Power = -12dBFS (Note 6)	Second Harmonic Distortion (Note 4)		-66.8	-55.4	dBc
			Third Harmonic Distortion (Note 4)		-67.7	-60.4	
Noise Density	ND	CW tone at 1842.5MHz, -15dBFS, measured at 10MHz offset from carrier, in 200kHz bandwidth			-157.5		dBm/Hz
DAC RESPONSE CHARACTERISTIC							
Output Power (CW) (Note 7)	P_{OUT}	0dBFS CW tone at DAC input, f_{OUT} = 100MHz	Excludes losses		3.2		dBm
			Excludes losses, includes sin(x)/x roll-off		3.2		
		0dBFS CW tone at DAC input, f_{DAC} = 5898.24Msps, f_{OUT} = 2140MHz	Excludes losses		0.4		
			Excludes losses, includes sin(x)/x roll-off		-2.5		
Output Bandwidth		f_{DAC} = 5898.24Msps, -1dB bandwidth, excludes losses (Note 7)			2600		MHz
Output Settling Time for Full-Scale Input Step (Note 8)		To ±0.024% of output full-scale in 4x interpolation mode			20		ns
INTERPOLATION FILTERS							
Interpolation Rates	R	Complex path			4x		
Passband Width	PBW	Ripple < 0.01dB			0.407 x f_{S_IN}		MHz
Stopband Rejection		4x interpolation, 0.593 x f_{S_IN}			80		dB
Data Latency (Excluding JESD204B Latency)		Interpolation bypass mode			372		DAC Clock Cycles
		4x interpolation			424		
NCO							
Maximum Frequency					f_{DAC}/2		Hz
Frequency Control Word Resolution					33		Bits

Electrical Characteristics (continued)

(V_{DD} = V_{AVCLK} = V_{AVDD} = $V_{AVDDPLL}$ = 1.0V, V_{DD2} = V_{AVCLK2} = V_{AVDD2} = $V_{AVDD2PLL}$ = V_{DD2PLL} = 1.8V, P_{CLK} = 0dBm, f_{CLK} = 983.04MHz, f_{DAC} = 4915.2Msps, 4x interpolation, 5-lanes, 9830.4Mbps per lane, external reference at 1.206V, R_{SET} = 965Ω between FSADJ and DACREF, I_{OUTFS} = 40mA, output is 50Ω double-terminated and transformer coupled (see Figure 26), PLL ON. T_A ≥ -40°C and T_J ≤ +110°C (Note 1), unless otherwise noted. Typical values are at T_J = +65 ±15°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
REFERENCE (REFIO)						
Reference Input Range			1.1		1.3	V
Reference Output Voltage	V_{REFIO}	Internal reference	1.1	1.2	1.3	V
Reference Input Resistance	R_{REFIO}			10		kΩ
Reference Voltage Drift				±110		ppm/°C
CMOS LOGIC INPUTS/OUTPUTS (SCLK, CSB, MUTE, RESETB, SDI, SDO, INTB)						
Input High Voltage	V_{IH}		0.7 x V_{DD2}			V
Input Low Voltage	V_{IL}				0.3 x V_{DD2}	V
Input Current	I_{IN}	Excluding RESETB	-1	±0.1	1	µA
RESETB Input Current	I_{INRB}		-1		55	µA
Input Capacitance	C_{IN}			3		pF
Output High Voltage	V_{OH}	I_{LOAD} = 200µA, INTB has a 1kΩ pullup resistor to V_{DD2}	0.8 x V_{DD2}			V
Output Low Voltage	V_{OL}	I_{SINK} = 200µA, INTB has a 1kΩ pullup resistor to V_{DD2}			0.2 x V_{DD2}	V
Output Leakage Current		Three-state, SDO pin	-4	±2.5	+4	µA
JESD204B INPUTS (DP5-DP0, DN5-DN0)						
Differential Input Return Loss	RL_{DIFF}			8		dB
Common-mode Input Return Loss	RL_{CM}			6		dB
Receiver Differential Resistance	R_{RxDIFF}	At DC	80		120	Ω
Minimum Differential Input Voltage	V_{MIN_IN}			110		mVp-p
Maximum Differential Input Voltage	V_{MAX_IN}			1050		mVp-p
Discrete Serial Data Rate per Lane	f_{SER_IN}	Also supports 1/2 and 1/4 fractional data rates		9830.4		Mbps
		Also supports 1/2 fractional data rates		7372.8		
		Also supports 1/2 fractional data rates		6144.0		
LVDS LOGIC OUTPUT (SYNCNP, SYNCNN, RCLKP, RCLKN)						
Differential Output Logic-High Voltage	V_{OH}	R_{LOAD} = 100Ω differential	250		450	mV
Differential Output Logic-Low Voltage	V_{OL}	R_{LOAD} = 100Ω differential	-450		-250	mV
Output Common Mode Voltage	V_{OCM}		1.125	1.25	1.375	V
Output Maximum Frequency	f_{RCLK}	R_{LOAD} = 100Ω differential, C_{LOAD} = 5pF		737.28		MHz

Electrical Characteristics (continued)

(V_{DD} = V_{AVCLK} = V_{AVDD} = $V_{AVDDPLL}$ = 1.0V, V_{DD2} = V_{AVCLK2} = V_{AVDD2} = $V_{AVDD2PLL}$ = V_{DD2PLL} = 1.8V, P_{CLK} = 0dBm, f_{CLK} = 983.04MHz, f_{DAC} = 4915.2Msps, 4x interpolation, 5-lanes, 9830.4Mbps per lane, external reference at 1.206V, R_{SET} = 965Ω between FSADJ and DACREF, I_{OUTFS} = 40mA, output is 50Ω double-terminated and transformer coupled (see Figure 26), PLL ON. T_A ≥ -40°C and T_J ≤ +110°C (Note 1), unless otherwise noted. Typical values are at T_J = +65 ±15°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
CLOCK INPUT (CLKP, CLKN)						
Power Level at Differential CLKP/CLKN Clock Input (Note 6)	P_{CLK}	Sine-wave input, PLL OFF		> 0		dBm
		Sine-wave input, PLL ON		> -3		
Common-Mode Voltage	V_{COM}	AC-coupled, internally biased		0.5		V
Differential Input Resistance	R_{CLK}			100		Ω
INTERNAL DAC CLOCK PLL						
Internal DAC Clock PLL Frequency Range	f_{PLL}	Low-band VCO frequency	4423.68		4915.20	MHz
		High-band VCO frequency	5898.24		6144.00	
PLL Input Frequencies	f_{CLK}	(Note 9)		f_{PLL}/MLT		MHz
Minimum PLL Input Frequency Multiplier	MLT_{MIN}			2		
Maximum PLL Input Frequency Multiplier	MLT_{MAX}			24		
Phase Noise at 6MHz Offset		f_{DAC} = 4915.2Msps, simulated at PLL output, does not include DAC core phase noise		-142		dBc/Hz
Cycle-to-Cycle Jitter		f_{DAC} = 4915.2Msps, simulated at PLL output, does not include DAC core jitter		245		fs
RESET TIMING						
RESET to Ready Delay	t_{RRDY}			350000		f_{CLK} Cycles
SERIAL PORT INTERFACE (Note 9)						
SCLK Frequency	f_{SCLK}	$1/t_{SCLK}$			20	MHz
SCLK to CSB Falling Edge Setup Time	t_{CSS}			10		ns
Minimum SCLK to CSB Falling Edge Hold Time	t_{CSH}			40		ns
Minimum SCLK Falling Edge to CSB Rising Edge Hold Time	t_{CRH}			$48/f_{DAC}$		ns
SDI to SCLK Hold Time	t_{SDH}	Data-write		0		ns
SDI to SCLK Setup Time	t_{SDS}	Data-write		5		ns
Minimum SCLK to SDO Data Delay	t_{SDD_MIN}	Data-read, 10pF load from SDO to Ground		1.5		ns
		Data-read, 100pF load from SDO to Ground		3.5		
Maximum SCLK to SDO Data Delay	t_{SDD_MAX}	Data-read, 10pF load from SDO to Ground		8		ns
		Data-read, 100pF load from SDO to Ground		11		
POWER SUPPLY						
1.0V Supply Voltage Range	V_{DD}, V_{AVDD}, $V_{AVDDPLL}$		0.95	1.0	1.05	V

Electrical Characteristics (continued)

(V_{DD} = V_{AVCLK} = V_{AVDD} = $V_{AVDDPLL}$ = 1.0V, V_{DD2} = V_{AVCLK2} = V_{AVDD2} = $V_{AVDD2PLL}$ = V_{DD2PLL} = 1.8V, P_{CLK} = 0dBm, f_{CLK} = 983.04MHz, f_{DAC} = 4915.2Msps, 4x interpolation, 5-lanes, 9830.4Mbps per lane, external reference at 1.206V, R_{SET} = 965Ω between FSADJ and DACREF, I_{OUTFS} = 40mA, output is 50Ω double-terminated and transformer coupled (see Figure 26), PLL ON. T_A ≥ -40°C and T_J ≤ +110°C (Note 1), unless otherwise noted. Typical values are at T_J = +65 ±15°C.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
1.0V Supply Voltage Range	V_{AVCLK}	f_{DAC} sample rate ≤ 4.9152Gsps		0.95	1.0	1.05	V
	V_{AVCLK}	f_{DAC} sample rate > 4.9152Gsps and ≤ 5.89824Gsps		1.00	1.02	1.05	
1.8V Supply Voltage Range	V_{DD2}, V_{AVCLK2}, V_{AVDD2}, $V_{AVDD2PLL}$, V_{DD2PLL}			1.71	1.8	1.89	V
1.0V Digital Supply Current	I_{VDD}	(Note 3)	4x Interpolation mode		550	750	mA
			Interpolation bypass mode, f_{DAC} = 2949.12MHz, JESD204B lanes = 6		500		
1.8V Digital Supply Current	I_{VDD2}	(Note 3)			500	550	mA
1.0V Clock Supply Current	I_{AVCLK}				350	400	mA
1.8V Clock Supply Current	I_{AVCLK2}				51	60	mA
1.0V Analog Supply Current	I_{AVDD}				230	270	mA
1.8V Analog Supply Current	I_{AVDD2}				270	295	mA
1.0V Clock PLL Supply Current	$I_{AVDDPLL}$				7	15	mA
1.8V Clock PLL Supply Current	$I_{AVDD2PLL}$				28	35	mA
1.8V JESD204B PLL Supply Current	$I_{VDD2PLL}$				27	35	mA
Total Power Dissipation	P_{TOTAL}	(Note 3)	4x Interpolation mode		2700	3100	mW
			Interpolation bypass mode, f_{DAC} = 2949.12MHz, JESD204B lanes = 6		2400		

Note 1: All specifications are guaranteed by test at T_J = +60°C and T_J = +115°C to an accuracy of ±10°C, unless otherwise noted. Specifications at T_J < +60°C are guaranteed by design and characterization. Timing specifications are guaranteed by design and characterization.

Note 2: Adjusted DAC update rate is defined as the rate at which the digital signal is converted to an analog signal and the output analog values are changed by the DAC. For DACs where the interpolation mode may be bypassed (interpolation factor of one), the DAC should be considered as a conventional (non-interpolating) DAC.

Note 3: Eight 6MHz 256-QAM carriers, f_{OUT} = 575MHz, Average Total Power = -12dBFS, input power is referenced to a 50Ω load.

Note 4: Specification guaranteed by design and characterization and functionally tested during production.

Note 5: Adjacent channel is 750kHz from channel block edge to 6MHz from channel block edge; next-adjacent channel is 6MHz from channel block edge to 12MHz from channel block edge; third-adjacent channel is 12MHz from channel block edge to 18MHz from channel block edge.

Note 6: Input power is referenced to a 50Ω load.

Note 7: Excludes losses from cables and matching network at DAC output, also excludes sin(x)/x roll-off unless otherwise noted.

Note 8: Settling time is dominated by the interpolation filter step response.

Note 9: DAC PLL reference input frequency multiplier (MLT), is defined by the ratio of the PLL feedback divide value (M) and the input reference divide value (N). MLT = M ÷ N, where M can be 16, 20, 24, 28, 32, 36, 40, 44, 48, 52, 56, or 60 and N can be 1, 2, 4, or 8, consistent with valid configurations listed in Table 9 and Table 10.

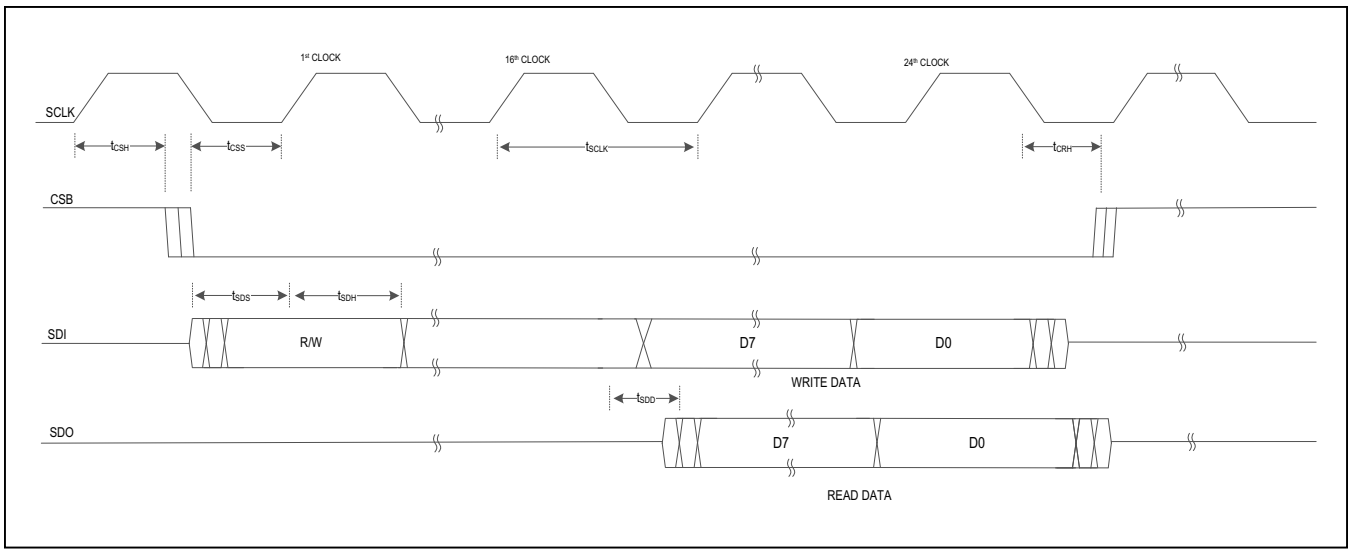
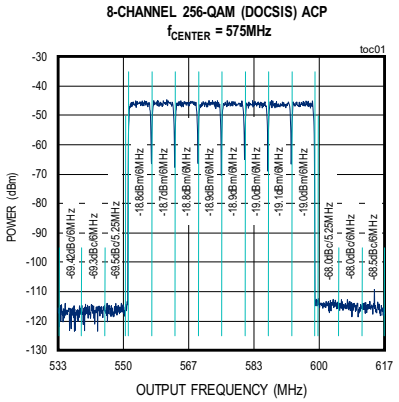
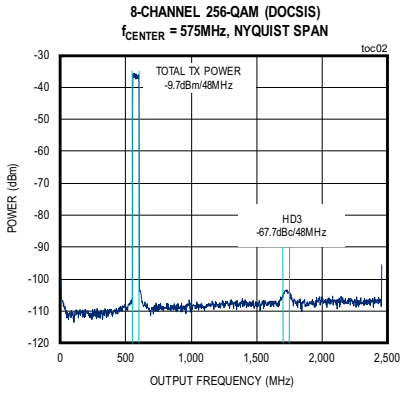


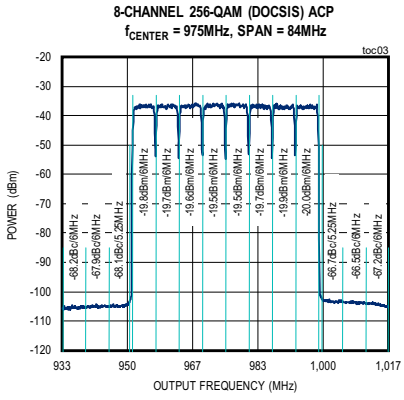
Figure 1. Serial Interface Timing Diagram

Typical Operating Characteristics

$V_{DD} = V_{AVCLK} = V_{AVDD} = V_{AVDDPLL} = 1.0V$, $V_{DD2} = V_{AVCLK2} = V_{AVDD2} = V_{AVDD2PLL} = V_{DD2PLL} = 1.8V$, $P_{CLK} = 0dBm$, $f_{CLK} = 983.04MHz$, f_{DAC} = 4915.2Msps, 4x interpolation, 5-lanes, 9830.4Mbps per lane, external reference at 1.20625V, R_{SET} = 965Ω between FSADJ and DACREF, I_{OUTFS} = 40mA, output is 50Ω double-terminated and transformer coupled (see Figure 26), PLL ON. $T_A \geq -40°C$ and $T_J \leq +110°C$ (Note 1), unless otherwise noted. Typical values are at T_J = +65 ±15°C.



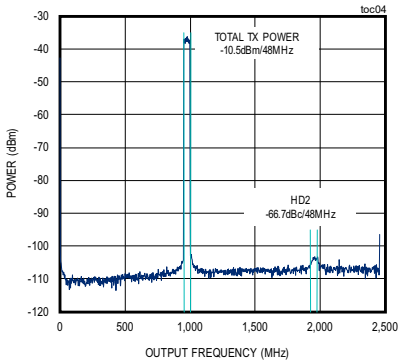




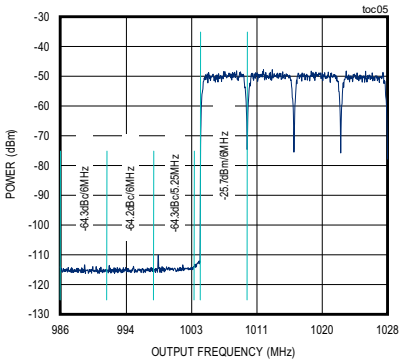
Typical Operating Characteristics (continued)

$V_{DD} = V_{AVCLK} = V_{AVDD} = V_{AVDDPLL} = 1.0V$, $V_{DD2} = V_{AVCLK2} = V_{AVDD2} = V_{AVDD2PLL} = V_{DD2PLL} = 1.8V$, $P_{CLK} = 0dBm$, $f_{CLK} = 983.04MHz$, f_{DAC} = 4915.2Msps, 4x interpolation, 5-lanes, 9830.4Mbps per lane, external reference at 1.20625V, R_{SET} = 965Ω between FSADJ and DACREF, I_{OUTFS} = 40mA, output is 50Ω double-terminated and transformer coupled (see Figure 26), PLL ON. $T_A \geq -40°C$ and $T_J \leq +110°C$ (Note 1), unless otherwise noted. Typical values are at T_J = +65 ±15°C.

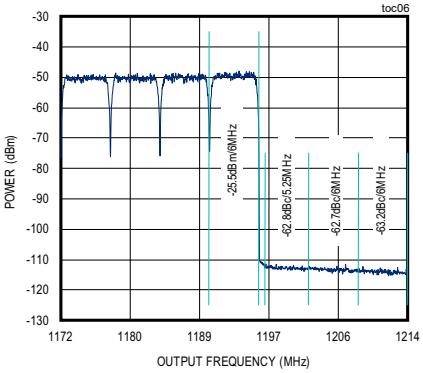
8-CHANNEL 256-QAM (DOCSIS)
f_{CENTER} = 975MHz, NYQUIST SPAN



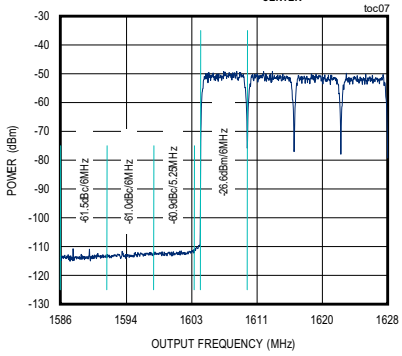
32-CHANNEL 256-QAM (DOCSIS) ACP
LOWER BLOCK EDGE, BLOCK f_{CENTER} = 1100MHz



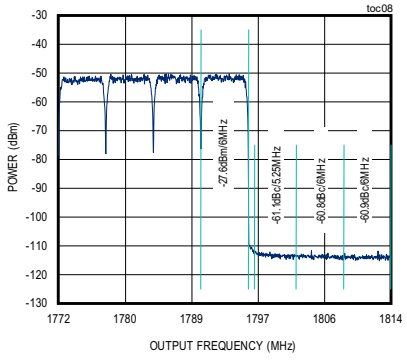
32-CHANNEL 256-QAM (DOCSIS) ACP
UPPER BLOCK EDGE, BLOCK f_{CENTER} = 1100MHz



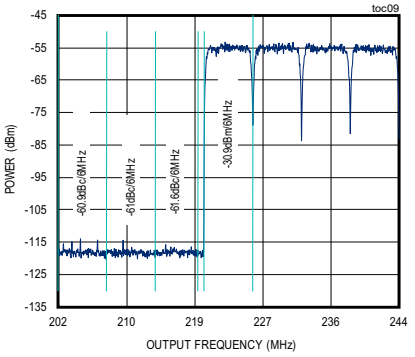
32-CHANNEL 256-QAM (DOCSIS) ACP
LOWER BLOCK EDGE, BLOCK f_{CENTER} = 1700MHz



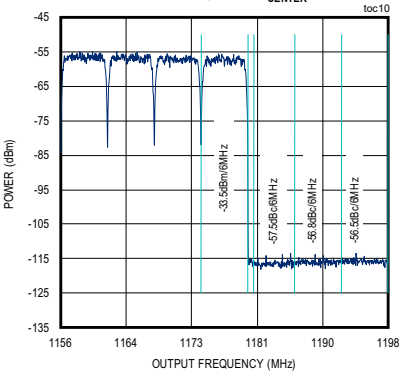
32-CHANNEL 256-QAM (DOCSIS) ACP
UPPER BLOCK EDGE, BLOCK f_{CENTER} = 1700MHz



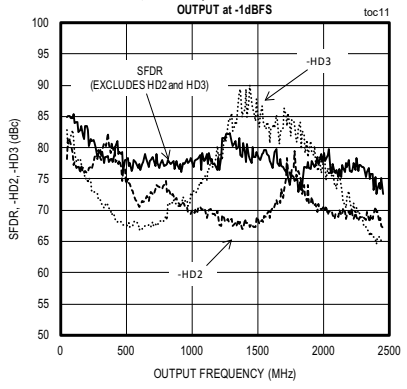
160-CHANNEL 256-QAM (DOCSIS) ACP
LOWER BLOCK EDGE, BLOCK f_{CENTER} = 700MHz



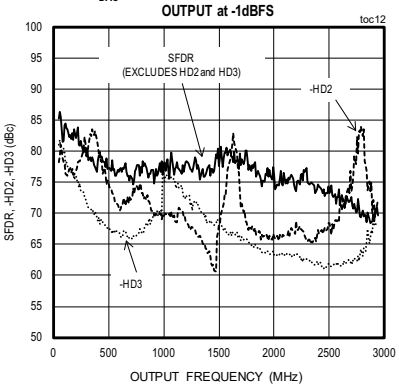
160-CHANNEL 256-QAM (DOCSIS) ACP
UPPER BLOCK EDGE, BLOCK f_{CENTER} = 700MHz



SFDR, HD2, HD3 vs. CW FREQUENCY
f_{DAC} = 4.9152Gsps, CONTINUOUS WAVE
OUTPUT at -1dBFS

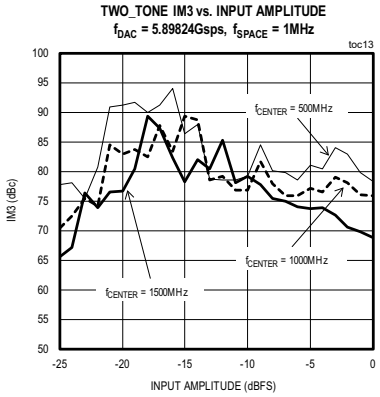


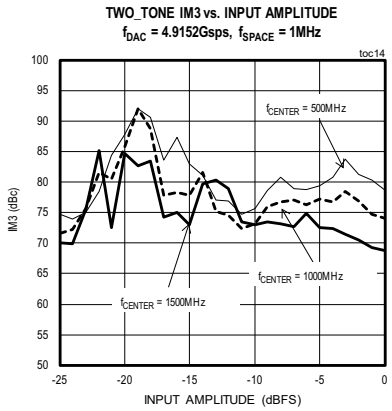
SFDR, HD2, HD3 vs. CW FREQUENCY
f_{DAC} = 5.89824Gsps, CONTINUOUS WAVE
OUTPUT at -1dBFS

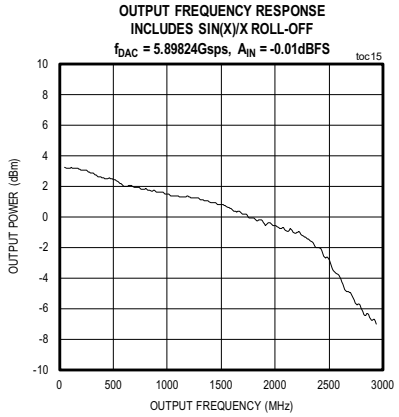


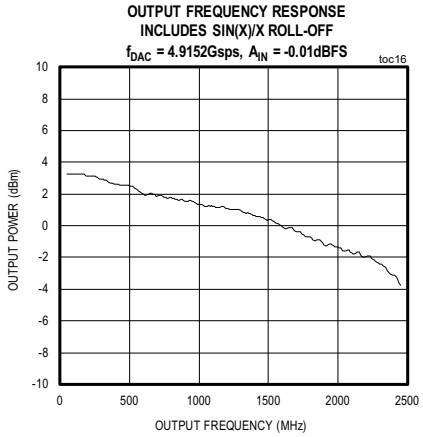
Typical Operating Characteristics (continued)

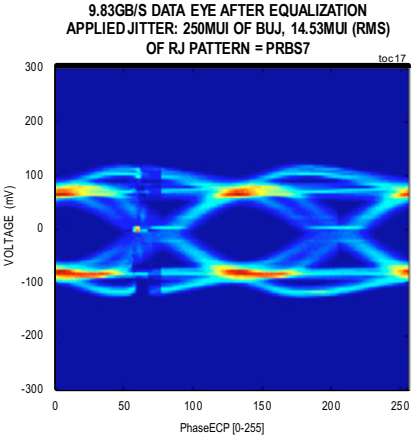
$V_{DD} = V_{AVCLK} = V_{AVDD} = V_{AVDDPLL} = 1.0V$, $V_{DD2} = V_{AVCLK2} = V_{AVDD2} = V_{AVDD2PLL} = V_{DD2PLL} = 1.8V$, $P_{CLK} = 0dBm$, $f_{CLK} = 983.04MHz$, f_{DAC} = 4915.2Msps, 4x interpolation, 5-lanes, 9830.4Mbps per lane, external reference at 1.20625V, R_{SET} = 965Ω between FSADJ and DACREF, I_{OUTFS} = 40mA, output is 50Ω double-terminated and transformer coupled (see Figure 26), PLL ON. $T_A \geq -40°C$ and $T_J \leq +110°C$ (Note 1), unless otherwise noted. Typical values are at T_J = +65 ±15°C.

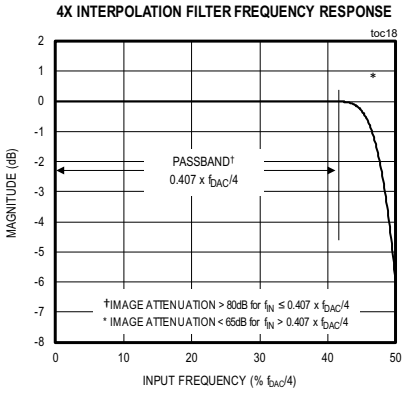


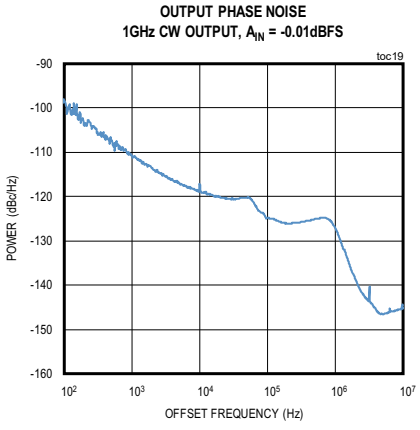




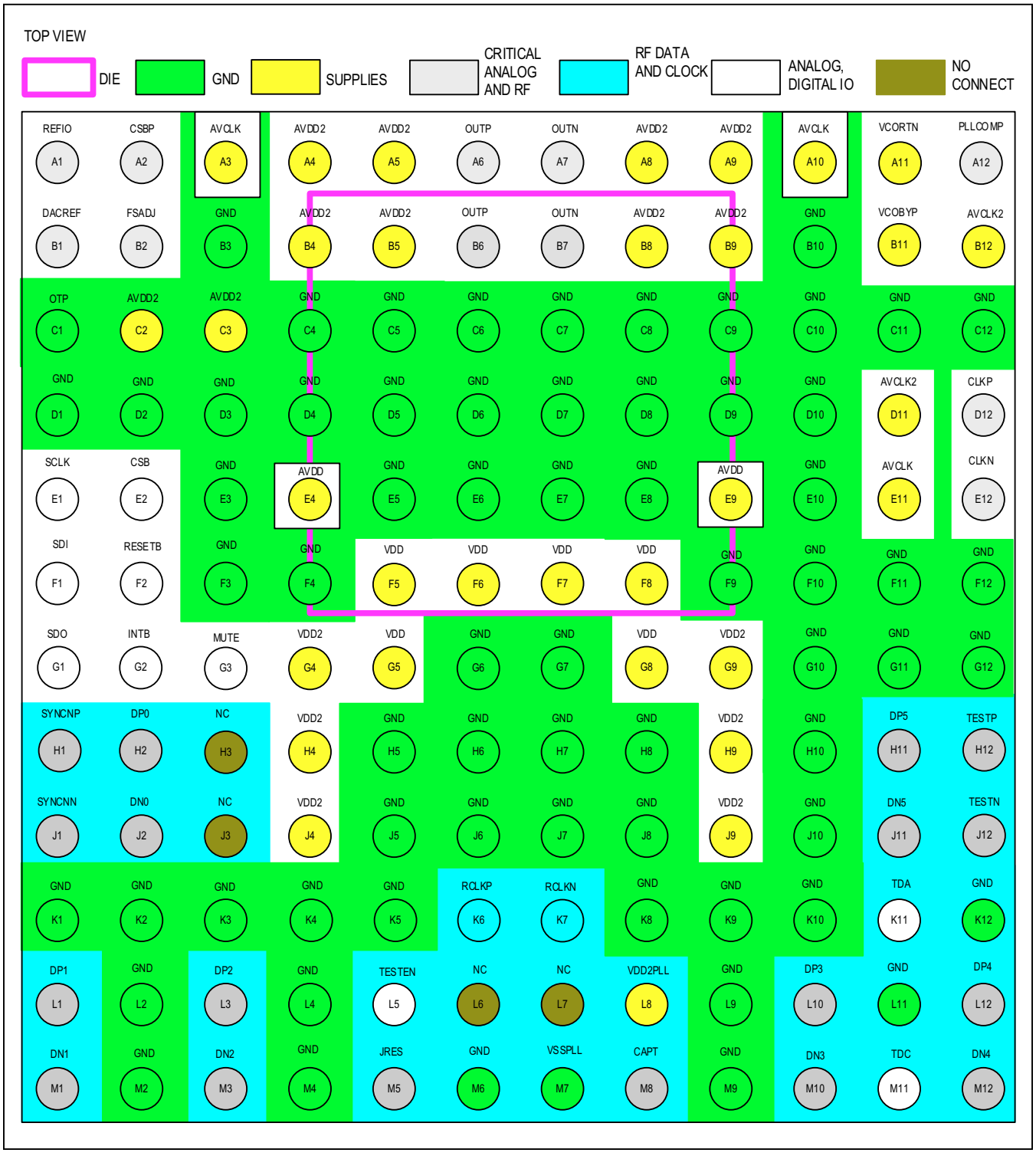








Pin Configuration



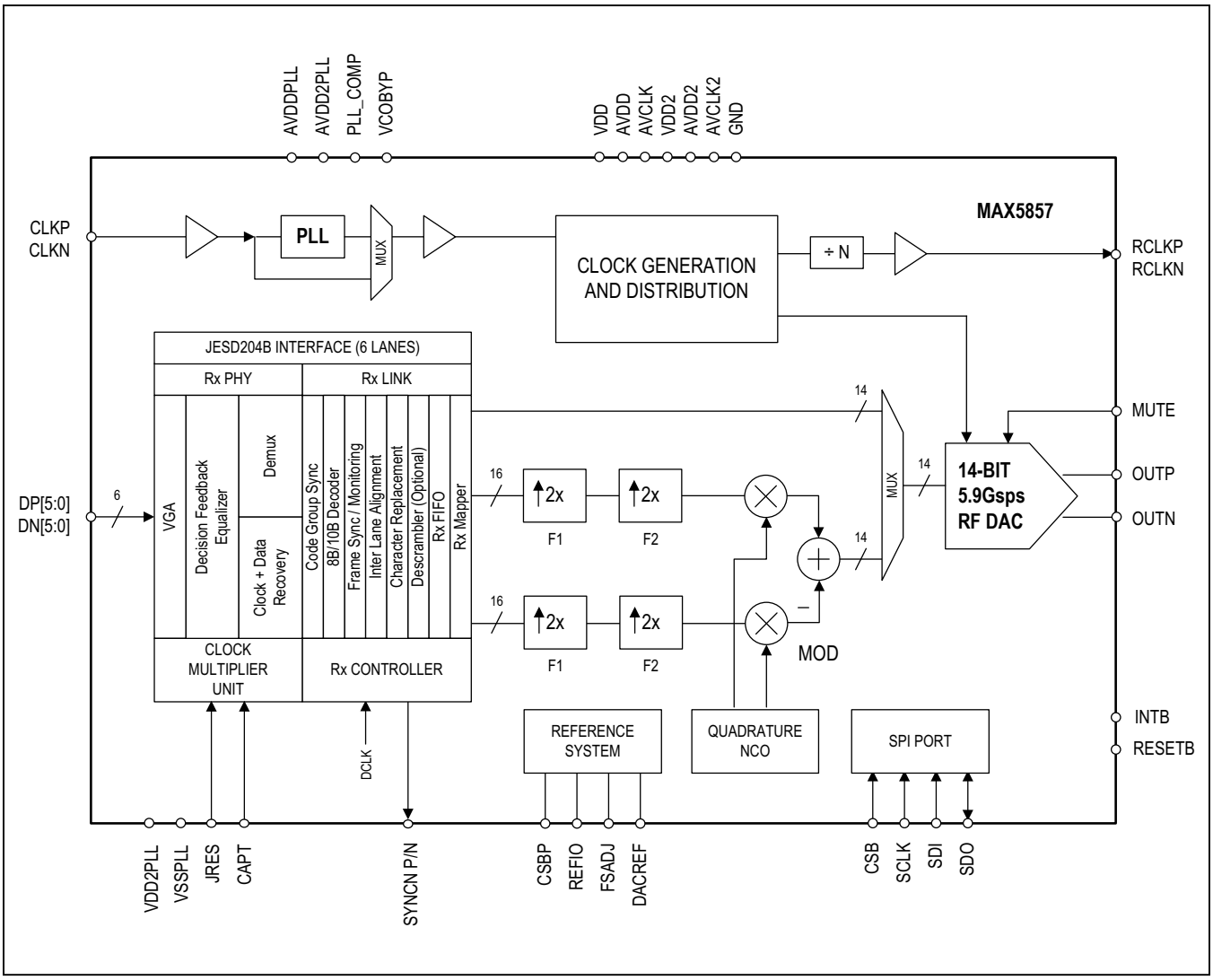
Pin Description

PIN	NAME	FUNCTION
A1	REFIO	Reference Voltage Input/Output. REFIO outputs an internal 1.2V band-gap reference voltage. REFIO has a 10kΩ series resistance and can be driven using an external 1.2V reference voltage. Connect a 1µF capacitor between REFIO and DACREF.
A2	CSBP	DAC Current Source Bypass. Connect 1.0µF capacitor between CSBP and DACREF.
A3, A10	AVCLK	1.0V Supply Input for Clock
A4-A5, A8-A9, B4-B5, B8-B9, C2-C3	AVDD2	Analog 1.8V Supply Input
A6, B6	OUTP	Positive Terminal of Differential DAC Output
A7, B7	OUTN	Negative Terminal of Differential DAC Output
A11	VCORTN	Ground for VCO Loop Filter
A12	PLLCOMP	Analog I/O for DAC PLL Loop Filter Connection
B1	DACREF	Internal DAC Reference Ground Used for DAC Current Source Bypass Ground. Do not connect to board ground (GND).
B2	FSADJ	Analog Input for DAC Full-Scale Output Current Adjustment. A resistor from FSADJ to DACREF sets the full-scale output current of the DAC. To obtain a 40mA full-scale output current using the internal reference voltage, connect a 965Ω resistor between FSADJ and DACREF.
B3, B10, C1, C4-C12, D1-D10, E3, E5-E8, E10, F3-F4, F9-F12, G6-G7, G10-G12, H5-H8, H10, J5-J8, J10, K1-K5, K8-K10, K12, L2, L4, L9, L11, M2, M4, M6, M9	GND	Ground
B11	VCOBYP	Pin for VCO Loop Filter
B12	AVCLK2	1.8V Supply Input for Clock
D11	AVDD2PLL	1.8V DAC Clock PLL Supply
D12, E12	CLKP, CLKN	Clock Input. Multipurpose pin that generates following internal clocks based on use case: 1) PLL use cases a) PLL OFF (Bypassed): Clock for RF DAC core (DACCLK) b) PLL ON (Enabled): Reference clock for DAC PLL which in turn generates the DACCLK 2) Device clock (DCLK) for JESD204B interface when frequency is ≤ 1474.56MHz in Subclass-0 operation An internal 100Ω termination resistor connects CLKP to CLKN.

Pin Description (continued)

PIN	NAME	FUNCTION
E1	SCLK	Digital CMOS Input for Serial Port Interface Clock
E2	CSB	Digital CMOS Input for Serial Port Interface. MAX5857 is selected when CSB = low.
E4, E9	AVDD	Analog 1.0V Supply Input
E11	AVDDPLL	1.0V DAC Clock PLL Supply
F1	SDI	Digital CMOS Input/Output for Serial Port Interface. Data input in 4-wire SPI mode and data input/output in 3-wire SPI mode.
F2	RESETB	Digital CMOS Input with an Internal 50kΩ Pulldown Resistor. Device is reset when RESETB is low. Hold RESETB low during device startup. RESETB must be set high for normal operation after startup.
F5-F8, G5, G8	VDD	1.0V Supply Input for Digital Core
G1	SDO	Digital CMOS Output for Serial Port Interface. Data output in 4-wire SPI mode.
G2	INTB	Digital CMOS Output for Interrupt
G3	MUTE	Digital CMOS Input. With MUTE high the DAC output is muted and with MUTE low, the DAC output is active.
G4, G9, H3-H4, H9, J3-J4, J9	VDD2	1.8V Supply Input for Digital I/O
H1, J1	SYNCNP, SYNCNN	LVDS Output. Active-low JESD204B error reporting signal (SYNC~) from Rx device (DAC) to Tx device (FPGA/ASIC).
H2, H11, L1, L3, L10, L12	DP0-DP5	Analog Input. JESD204B Serial Data Positive Input, Lanes 0-5
H3, J3, L6, L7	NC	No Connect
H12, J12	TESTP, TESTN	Factory Use Only. Connect to GND.
J2, J11, M1, M3, M10, M12	DN0-DN5	Analog Input JESD204B Serial Data Negative Input, Lanes 0-5.
K6-K7	RCLKP, RCLKN	LVDS Reference Clock Output for Sample Rate Synchronization to DAC Clock. If not used, terminate differential with a 100Ω resistor.
K11	TDA	Temperature Sensor Diode Anode. Connect TDC and TDA to ground if not used.
L5	TESTEN	Factory Use Only. Connect to GND.
L8	VDD2PLL	JESD204B PLL 1.8V Power Supply
M5	JRES	Analog Input. JESD204B current biasing.
M7	VSSPLL	Clock Multiplier Unit (CMU) PLL Ground
M8	CAPT	Analog Input. JESD204B PLL loop filter input.
M11	TDC	Temperature Sensor Diode Cathode. Connect TDC and TDA to ground if not used.

Functional Diagram



Detailed Description

The MAX5857 is a high-performance interpolating and modulating 14-bit, 5.9Gsps RF DAC designed for DOCSIS 3.1 remote PHY devices, CCAP, digital video broadcast modulators, point-to-point wireless, and instrumentation. The device can synthesize up to 1.2GHz of instantaneous bandwidth at frequencies up to the Nyquist bandwidth ($f_{DAC}/2$) of the DAC. The major functional blocks of the device include a six-lane JESD204B interface which accepts 16-bit input data, interpolation filters, a digital quadrature modulator and NCO, clock multiplying PLL+VCO and a 14-bit, 5.9Gsps RF DAC core. The supporting functional blocks include the clock distribution system, reference system, and SPI interface. See the detailed *Functional Diagram*.

The 16-bit input data enhances the accuracy of the interpolation and modulation functions and ensures true 14-bit data is presented to the RF DAC core. The 16-bit input baseband data is supplied to the device using up to six lanes of JESD204B (DP[5:0]/DN[5:0]). The interface can be configured for 3, 4, 5, or 6 lanes and supports serial data rates up to 9.8304Gbps providing flexibility to optimize the I/O lane count, speed, and power to support the required frequency plan.

The six-lane JESD204B interface has the following major components:

- A high-speed input receiver (Rx) consisting of a physical (PHY) layer for each of the six lanes and a common clock multiplier unit (CMU). The PHY layer contains a variable gain amplifier (VGA) that receives the incoming signal and decision feedback equalizer (DFE) to suppress inter-symbol interference. The PHY layer also includes a clock and data recovery (CDR) unit to latch the incoming single-bit data and a de-serializer (DEMUX) to convert the data to a 20-bit parallel data bus.
- A receiver link layer (Rx Link) takes the 20 bits from the PHY and restores the 16-bit DAC data for each of the I and Q channels. The Rx link consists of six Rx lanes, six Rx FIFOs, a Rx mapper and a Rx controller. The six Rx lanes perform code group synchronization, 8b/10b decoding, frame synchronization and monitoring, interlane alignment and monitoring, character replacement, and optional descrambling. The six lanes are fed into Rx FIFOs where data is aligned by the Rx controller. Using the Rx mapper, data from each physical channel is mapped to a logical channel.

The DSP path consists 4x linear phase interpolation filters for each of the I and Q channels. Interpolation reduces the required input data rate to the device, relaxing the requirements on the FPGA or ASIC. In addition, interpolation increases the separation between the desired signal and its aliased image easing filter design requirements. Interpolation rates of 1x (bypass path) or 4x (complex path) can be selected using SPI configuration.

After passing through the 4x interpolation stage, the complex signal is modulated using the LO signal generated by the NCO and the digital quadrature modulator. The NCO allows for fully agile modulation of the input base-band signal for direct RF synthesis with 32 bits of frequency-setting resolution. Placing the modulator at the output of the interpolator chain allows for fully agile placement of the output carrier frequency within the Nyquist band of the DAC. The quadrature modulator produces a real signal at its output, which is fed into the 14-bit DAC core where it is converted to an analog RF signal. The analog output produces a full-scale current between 10mA and 40mA, driving 50Ω differential loads.

The clock distribution system provides a low-noise differential input buffer for the external master DAC clock (CLKP/CLKN) and delivers all the necessary clocks to the internal blocks. The master DAC clock input accepts a differential sine-wave or square-wave signal. A bypassable clock multiplying PLL and VCO can be used to internally generate, the high-frequency sampling clock using a reference frequency between 245.76MHz and 1.475GHz. The device provides a divided reference clock (RCLKP/RCLKN) to ensure synchronization between the data source (FPGA or ASIC) and the DAC. The SYNCN output can be used for error reporting from the DAC to the data source.

The reference system delivers the reference current to the DAC current source array and all bias currents necessary for circuit operation. The reference system also includes a bypassable band-gap reference, which can be used as a reference for the DAC full-scale current. The SPI port is a bidirectional interface used for reading and writing status and control registers to configure the device. The device operates from 1.0V and 1.8V power-supply voltages and consumes 2.7W at 4.9Gsps.

Supported DAC Update Rate and JESD204B Data Rates

Table 1. Complex I/Q Base Band Up-Conversion (4x Interpolation)

	DAC UPDATE RATE: DACCLK (MSPS)						
	2457.60	2949.12	3686.40	3932.16	4423.68	4915.20	5898.24
Input Sample Rate - I & Q each (MHz)	614.4	737.28	921.6	983.04	1105.92	1228.8	1474.56
Instantaneous Bandwidth (MHz)	500	600	750	800	900	1000	1200

Table 2. Lane Rate - Derived from Number of Lanes and Update Rate (DACCLK)

LANES	DACCLK (MSPS)						
	2457.60	2949.12	3686.40	3932.16	4423.68	4915.20	5898.24
	Lane Rate (Mbps)						
3	-	9830.4	-	-	-	-	-
4	6144.0	7372.8	-	9830.4	-	-	-
5	4915.2 9830.4*	-	-	-	-	9830.4	-
6	-	4915.2 9830.4*	6144.0	-	7372.8	-	9830.4

**Bypass Mode Rates*

Note that DAC update rates of 3686.40Msps and 3932.16Msps are not supported by the internal clock multiplying PLL+VCO. Use an external sampling clock for these DAC update rates. DAC update rates of 2457.60Msps and 2949.12Msps are supported by the internal clock multiplying PLL+VCO at 4915.20Msps and 5898.24Msps respectively using a Post Divider setting of 2.

JESD204B Interface

The JESD204B interface consists of six PHY lanes with one CMU. Each lane takes a 1-bit stream and converts it to a 20-bit bus. The link layer (LINK) takes the 20-bit bus from the PHY and restores the original 16-bit DAC data for each of the I and Q channels (Figure 2).

The JESD204B receiver specifications are compliant with LV-OIF-6G-SR and LV-OIF-11G-SR specifications from the JEDEC standard.

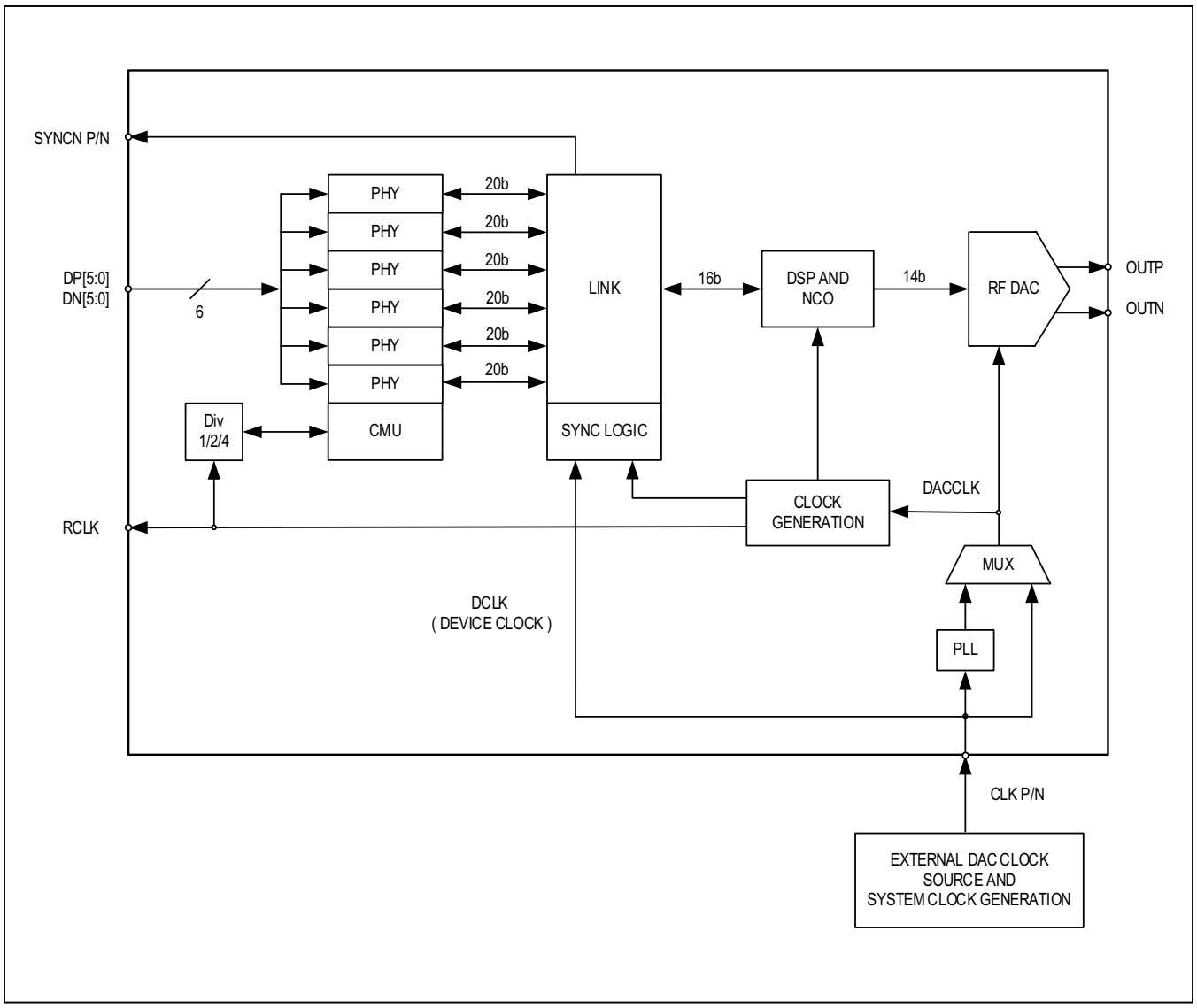


Figure 2. Simplified Diagram of JESD204B Internal to MAX5857

Table 3. JESD204B Power Dissipation

JESD LANES	TOTAL POWER (MW)
3	443
4	563
5	684
6	804

***Total Power** values are for PHY, CMU, and LINK blocks running at 7.3728Gbps/lane.*

JESD204B Data Interface Features

A summary of the MAX5857 PHY and LINK features is provided below:

Rx PHY Features

- Programmable gain

LINK Features

- 8b/10b decoding
- Code group synchronization
- Inter Lane Alignment (ILA)
- $1 + x^{14} + x^{15}$ polynomial scrambling
- Character replacement
- Multiple Converter Device Alignment-Multiple Lanes (MCDA-ML) compliant
- Subclass-0 support
- Number of lanes (L): 3, 4, 5, 6
- Number of data converters (M): 2
- Number of octets per frame (F): 2, 4
- Number of samples per frame (S): 2, 3, 5

Other Features

- Disable scramble mode
- Elastic buffer depth of 320 serial bit-periods
- Detection of following 8b/10b control characters: K28.0, K28.3, K28.4, K28.5, K28.7
- Detection of following errors/conditions
  - 8b/10b running disparity error
  - 8b/10b not-in-table error
  - Unexpected control character detection
  - Code group synchronization error
  - Frame re-alignment detection
  - Lane re-alignment detection
  - Link configuration error
  - ILA failure detection
  - ILA sequence error

Some of the above error conditions can be enabled for error reporting through SYNC~ interface.

- Continuous /K/ and ILA sequence detection
- PHY PRBS data detection for debug

Mapping of Physical to Logical Channels

Each physical channel can be mapped to any logical channel before the octet-to-sample conversion. The octet-to-sample conversion for various modes is determined by the number of lanes, number of octets per frame (JESD204B), and number of samples per frame, according to the formats shown in Figure 3.

Mapping of Bypass Mode Data

When bypassing the internal 4x interpolation filters and NCO modulator, the JESD lane interface is mapped for real-data only (samples) rather than I and Q octets. Figure 4 shows the lane mapping for the DSP Bypass data path. The DAC logical channel mapping is configured for MLFSN'=2_6_2_3_16 mode but is actually receiving data which is transmitted in 1_6_2_6_16 mode. Since the JESD transmitters and receivers are set to a mixed-mode lane configuration, a mismatch error will be detected and indicated in the RxLink.CfgRLaneMuteEn.LCfgErr register field for all lanes. This status should be ignored and not enabled for DAC Mute or Interrupt enable. For additional information see the *DSP Bypass Function Configuration* section.

High-Speed Input Receiver (Rx)

As shown in Figure 5, the high-speed input receiver consists of a VGA, DFE (Decision Feedback Equalizer), CDR unit, and DEMUX. The VGA and DFE provide autonomous adaptive equalization in order to optimize the input receiver filter coefficients on a per-lane basis. The coefficients are optimized to best recover the data dependent jitter introduced by the incoming channel. The initial receiver gain and equalization settings are shadowed by internal registers which the user may override.

The VGA is a high-speed input receiver with high gain, which allows for excellent input sensitivity while still preserving the linearity required for optimal performance of the DFE. The receiver expects the incoming high-speed signal to be driven differential and AC-coupled to the transmitter. The receiver's common-mode input voltage is set by a self-biasing network eliminating the need for any external board circuitry. The receiver provides 100Ω differential on-chip termination between the true and complement input signals, RxP and RxN. The VGA gain settings are based on the amplitude of the incoming signal and the optimal setting to the DFE circuitry; the gain range is ±20dB as shown in Figure 6. In addition to the gain function, there is also a boost function in the VGA to compensate for the high-frequency loss in the channel.

The PHY receiver automatically determines and sets the optimized level of equalization to suppress inter-symbol interference (ISI) caused by a dispersive channel known as decision feedback equalization. The DFE makes use of previously received data to estimate the current bit. Any trailing ISI caused by a previous bit is reconstructed and then subtracted. This technique allows for the recovery of very lossy backplane and connector channels. The PHY equalizer is designed to meet or exceed the JESD204B standard.

LANE 5	LANE 4	LANE 3	LANE 2	LANE 1	LANE 0	
Q_2[15:8]	Q_1[15:8]	Q_0[15:8]	I_2[15:8]	I_1[15:8]	I_0[15:8]	MLFSN'=2_6_2_3_16
Q_2[7:0]	Q_1[7:0]	Q_0[7:0]	I_2[7:0]	I_1[7:0]	I_0[7:0]	
Q_5[15:8]	Q_4[15:8]	Q_3[15:8]	I_5[15:8]	I_4[15:8]	I_3[15:8]	
Q_5[7:0]	Q_4[7:0]	Q_3[7:0]	I_5[7:0]	I_4[7:0]	I_3[7:0]	
	Q_3[15:8]	Q_1[15:8]	I_4[15:8]	I_2[15:8]	I_0[15:8]	MLFSN'=2_5_4_5_16
	Q_3[7:0]	Q_1[7:0]	I_4[7:0]	I_2[7:0]	I_0[7:0]	
	Q_4[15:8]	Q_2[15:8]	Q_0[15:8]	I_3[15:8]	I_1[15:8]	
	Q_4[7:0]	Q_2[7:0]	Q_0[7:0]	I_3[7:0]	I_1[7:0]	
	Q_8[15:8]	Q_6[15:8]	I_9[15:8]	I_7[15:8]	I_5[15:8]	
	Q_8[7:0]	Q_6[7:0]	I_9[7:0]	I_7[7:0]	I_5[7:0]	
	Q_9[15:8]	Q_7[15:8]	Q_5[15:8]	I_8[15:8]	I_6[15:8]	
	Q_9[7:0]	Q_7[7:0]	Q_5[7:0]	I_8[7:0]	I_6[7:0]	
		Q_1[15:8]	Q_0[15:8]	I_1[15:8]	I_0[15:8]	MLFSN'=2_4_2_2_16
		Q_1[7:0]	Q_0[7:0]	I_1[7:0]	I_0[7:0]	
		Q_3[15:8]	Q_2[15:8]	I_3[15:8]	I_2[15:8]	
		Q_3[7:0]	Q_2[7:0]	I_3[7:0]	I_2[7:0]	
			Q_1[15:8]	I_2[15:8]	I_0[15:8]	MLFSN'=2_3_4_3_16
			Q_1[7:0]	I_2[7:0]	I_0[7:0]	
			Q_2[15:8]	Q_0[15:8]	I_1[15:8]	
			Q_2[7:0]	Q_0[7:0]	I_1[7:0]	
			Q_4[15:8]	I_5[15:8]	I_3[15:8]	
			Q_4[7:0]	I_5[7:0]	I_3[7:0]	
			Q_5[15:8]	Q_3[15:8]	I_4[15:8]	
			Q_5[7:0]	Q_3[7:0]	I_4[7:0]	

Figure 3. Octet-to-Sample Conversion vs. Modes and Lanes

LANE 5	LANE 4	LANE 3	LANE 2	LANE 1	LANE 0	
S_5[15:8]	S_3[15:8]	S_1[15:8]	S_4[15:8]	S_2[15:8]	S_0[15:8]	MLFSN'=2_6_2_3_16
S_5[7:0]	S_3[7:0]	S_1[7:0]	S_4[7:0]	S_2[7:0]	S_0[7:0]	
	S_7[15:8]	S_3[15:8]	S_8[15:8]	S_4[15:8]	S_0[15:8]	MLFSN'=2_5_4_5_16
	S_7[7:0]	S_3[7:0]	S_8[7:0]	S_4[7:0]	S_0[7:0]	
	S_9[15:8]	S_5[15:8]	S_1[15:8]	S_6[15:8]	S_2[15:8]	
	S_9[7:0]	S_5[7:0]	S_1[7:0]	S_6[7:0]	S_2[7:0]	

Figure 4. Bypass Mode Sample to Lane Mapping

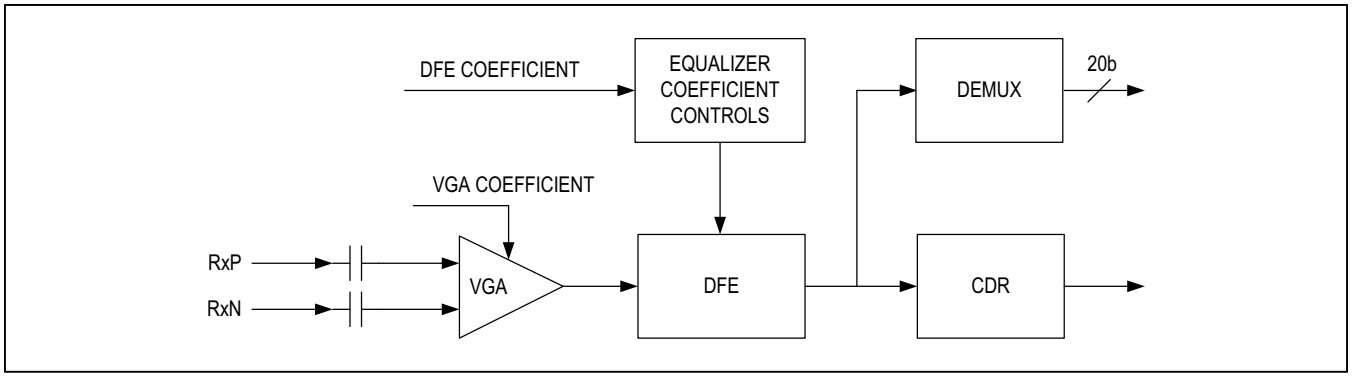


Figure 5. JESD204B Rx Physical Layer, Simplified Block Diagram

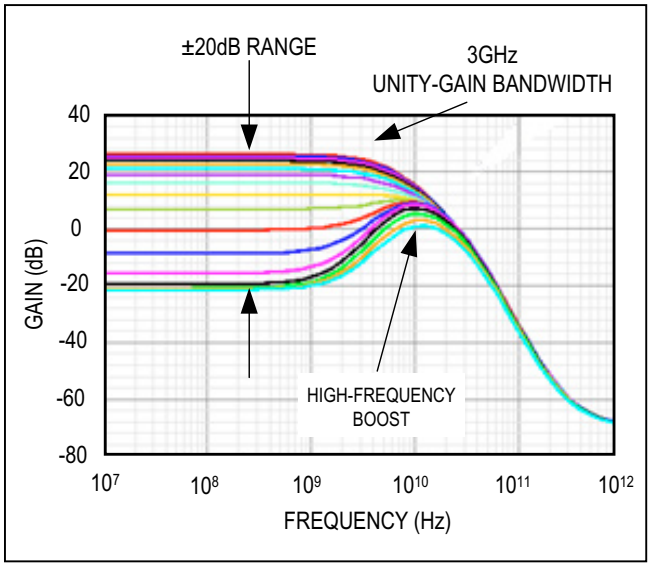


Figure 6. VGA Gain Range

The CDR unit is responsible for the centering of the incoming data eye for optimal sampling and error free operation. The PHY clock and data recovery unit has multiple loop bandwidth settings to aid in achieving optimal performance for jitter tolerance.

The recovered clock generated from CDR is used to latch in the single bit data, then the DEMUX block de-serializes the single bit to 20-bit parallel data bus to subsequently be used by the Rx LINK.

JESD204B Receiver Equalization

The MAX5857 JESD204B receiver equalization capability exceeds the JEDEC specification for maximum interconnect length of 20cm.

The plots in Figure 7 demonstrate that the JESD204B receiver equalization capability over a 30in (76cm) length of cable using the following test conditions:

- Data Rate: 9.8304Gbps
- Channel: 30in Nelco 4000-13SI plus cables and FMC connector
- 30in Nelco Traces = -14.7dB loss at 4.914GHz (see Figure 8)
- Cables and connector ~ 3dB loss at 4.914GHz

Lane Skew Requirement

The skew between the various lanes is absorbed within the FIFOs and through the initial lane alignment process. The FIFO depth determines the amount of lane skew that can be absorbed for a particular Rx LINK configuration. A FIFO depth of 32 bytes would account for up to 320 SerDes bit periods of skew between the various lanes. In actuality, the maximum supported skew is smaller than this due to multiple bytes written to and read from the FIFO in a single write/read clock cycle in various modes. The maximum supported skew is also reduced due to the write to read-clock synchronization uncertainty. A minimum and maximum FIFO depth can be set (CfgRFIFO at address 0x041C) and the configured FIFO range determines the actual lane skew supported by the MAX5857.

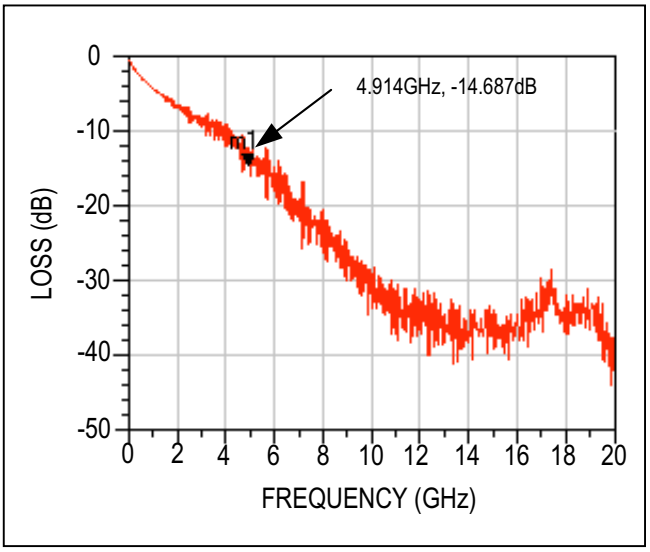


Figure 8. Channel Loss Curve (30in Nelco)

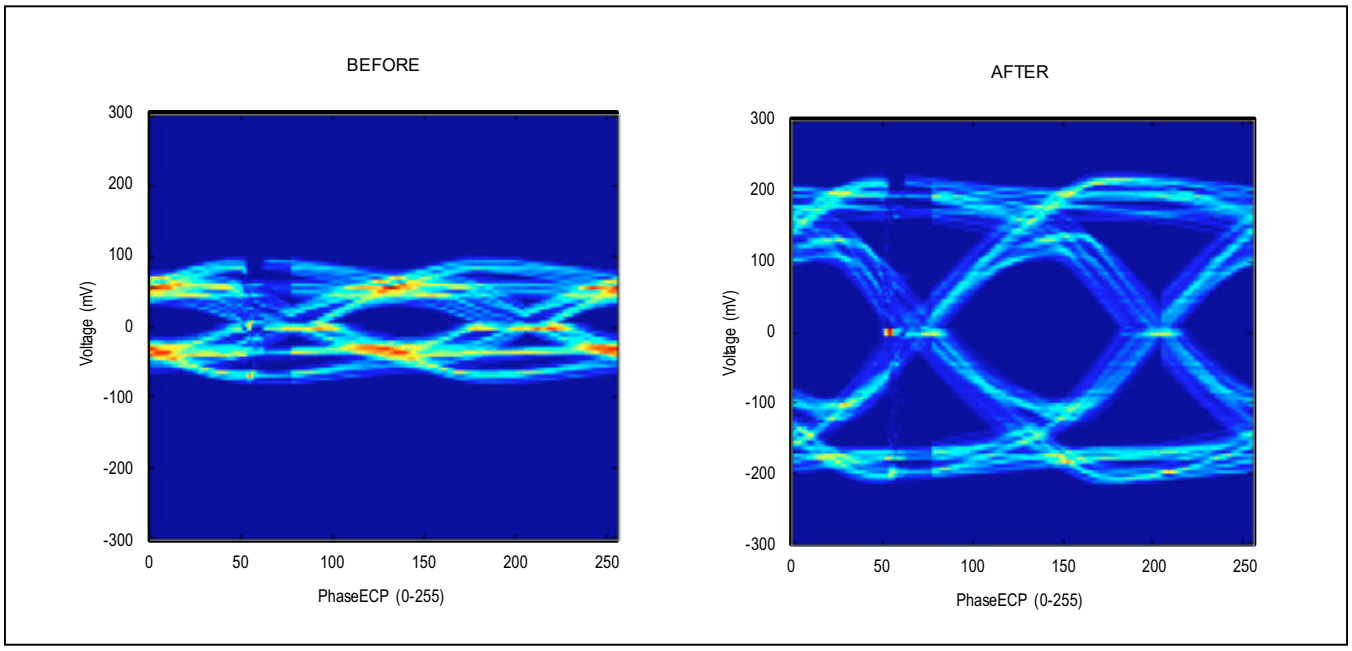


Figure 7. Receiver Equalization Eye Diagram Before and After Lane Training

Link Layer (LINK)

The Rx LINK layer for the MAX5857 consists of 6 lanes interfacing to the 6 PHYs. The data from the 6 lanes is passed through FIFOs in order to align the configured number of lanes in JESD204B Subclass-0 mode. The Rx controller generates a SYNCN signal for error reporting as specified by the JESD204B standard. The data from the FIFOs are then mapped into I and Q sample data for the DSP to process.

Each of the 6 lanes in the Rx LINK operates independently and includes code group synchronization operating on the 20-bit input from the PHY, 8b/10b decoding, frame synchronization and monitoring, lane alignment and monitoring, character replacement and optional descrambling. All these functions are specified in the JESD204B standard. In addition to extracting the octets, which are later combined into I and Q samples, the Rx LINK also monitors and acts on various error conditions. Most error conditions can be enabled for error reporting to the transmit logic service through the SYNCN signal. See Table 4 for more detail.

On the input side of the Rx LANE there are 20 bits of data and the CLOCK from the PHY, along with a synchronous RESET. On the output side are 16 bits of data (two octets), FRAME START, and MULTIFRAME START signals which mark the two bytes of data.

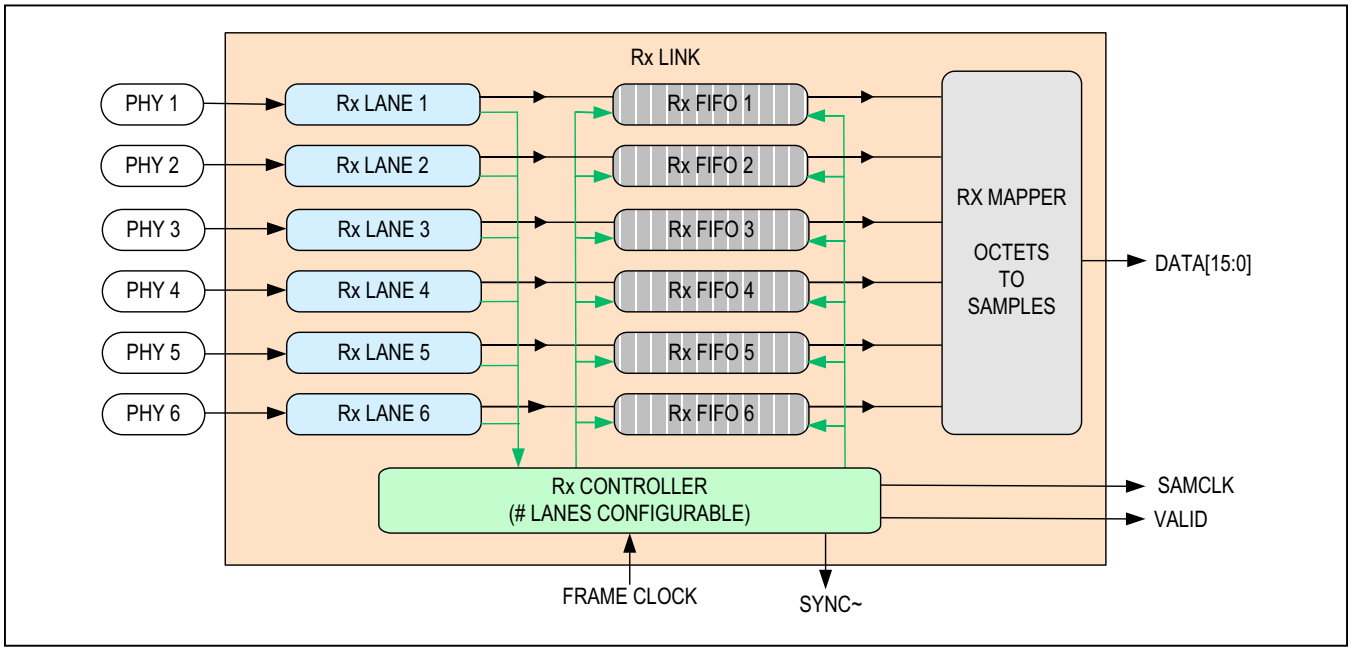


Figure 9. JESD204B Receive Link Layer Block Diagram

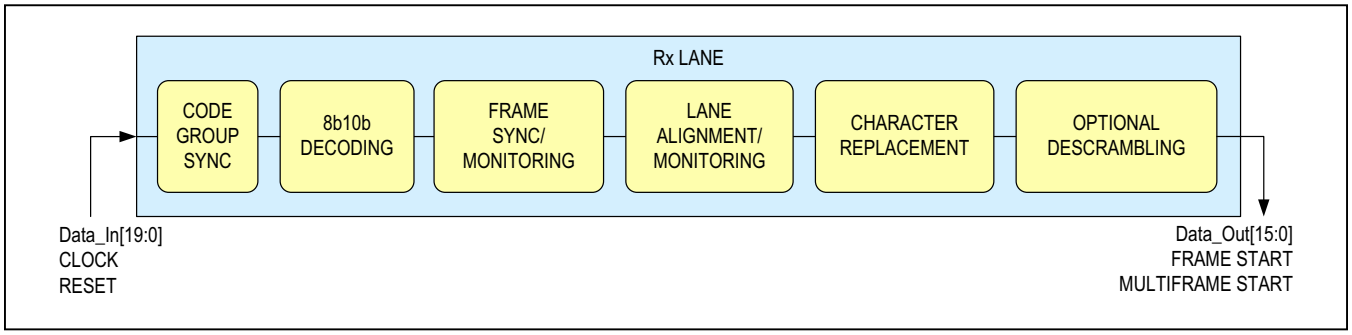


Figure 10. JESD204B Receive Lane Block Diagram

Interface Timing for Subclass-0

The JESD204B LINK layer protocol requires the frame clock of both the transmitter and receiver devices to be synchronized. Figure 11 shows the JESD204B-TX device's synchronization with the MAX5857 using the SYNCN signal. Initially, the internal clocks of the two devices are running independently. As shown, the SYNCN signal is generated by the MAX5857 using its frame clock, which in turn is used by the JESD204B-TX device to align its own frame clock.

The Rx Controller waits for the FIFO write to start in all the enabled lanes and then initiates a read start to all the FIFOs. The FIFO reads start at the Frame/Multiframe boundary following the lane alignment sequence. This process aligns the data on all enabled lanes with a minimum latency through the Rx LINK.

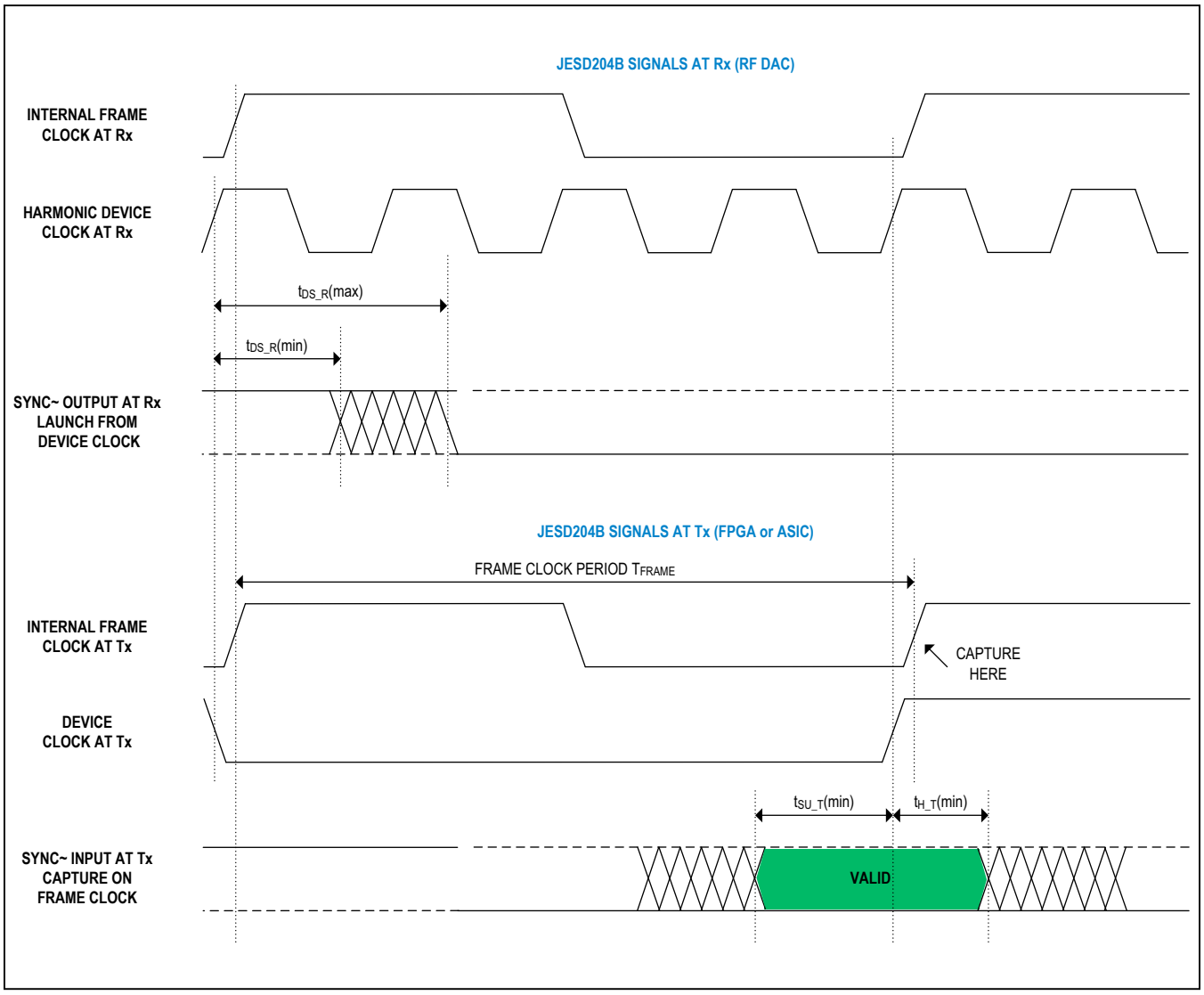


Figure 11. Interface Timing for Subclass-0 (See JEDEC Standard No. 204B.01, Figure 11)

Serial Control Interface

The serial control interface is comprised of the CSB, SCLK, SDI, and SDO pins which support a typical 4-wire SPI interface. It also supports a 3-wire SPI interface where the SDI pin acts as both digital data input and output, commonly referred to as SDIO.

The MAX5857 is always a slave device with the master controlling CSB, SCLK, and SDI. The SPI clock frequency must meet certain constraints for proper operation and response from the MAX5857. Refer to the *SPI to PCLK Frequency Ratio* section.

In 4-wire SPI interface mode, CSB, SCLK, and SDI are 1.8V CMOS-level digital input pins. SDO is a 1.8V CMOS output signal when the MAX5857 is transmitting serial data. SDO is a high-impedance output at all other times. CSB is the chip-select pin. While CSB is low, the MAX5857 device is open to communication through the SCLK, SDI, and SDO pins. Each communication cycle is comprised of a single read/write bit, a 15-bit address word, and an 8-bit data word. The serial interface clock, SCLK, latches data into the MAX5857 on the rising edge and clocks data out of the MAX5857 on the falling edge. A logic '1' for the R/W bit signifies a read operation and a logic '0' indicates a write operation.

The R/W bit and the address word are sent to the device through the SDI pin. The R/W bit is transmitted first, followed by the address word in MSB to LSB order while in the default MSB-first format. In the LSB-first format, the address word is transmitted first, LSB to MSB, followed by the R/W bit. Input or output data are transmitted MSB- or LSB-first order, based on the format setting. Further descriptions assume MSB-first format.

For a write operation, a data word is immediately written to the SDI after the last bit of the address. For a read operation, the data word is transmitted from the MAX5857 on the SDO signal line. The transmission starts on the falling edge of SCLK immediately after the last bit is latched into the device. The SDO driver enters a high-impedance state on the next falling SCLK edge immediately after the bit is transmitted. CSB must toggle from low to high and then back to low before another communication cycle can resume. An exception is burst mode operation.

When burst mode is enabled, a continued assertion of CSB after the data word will auto decrement/increment the address word depending on the configuration for a successive read/write. Every 8 cycles of SCLK will access a successive address for either write or a read based on the R/W bit in the initial command.

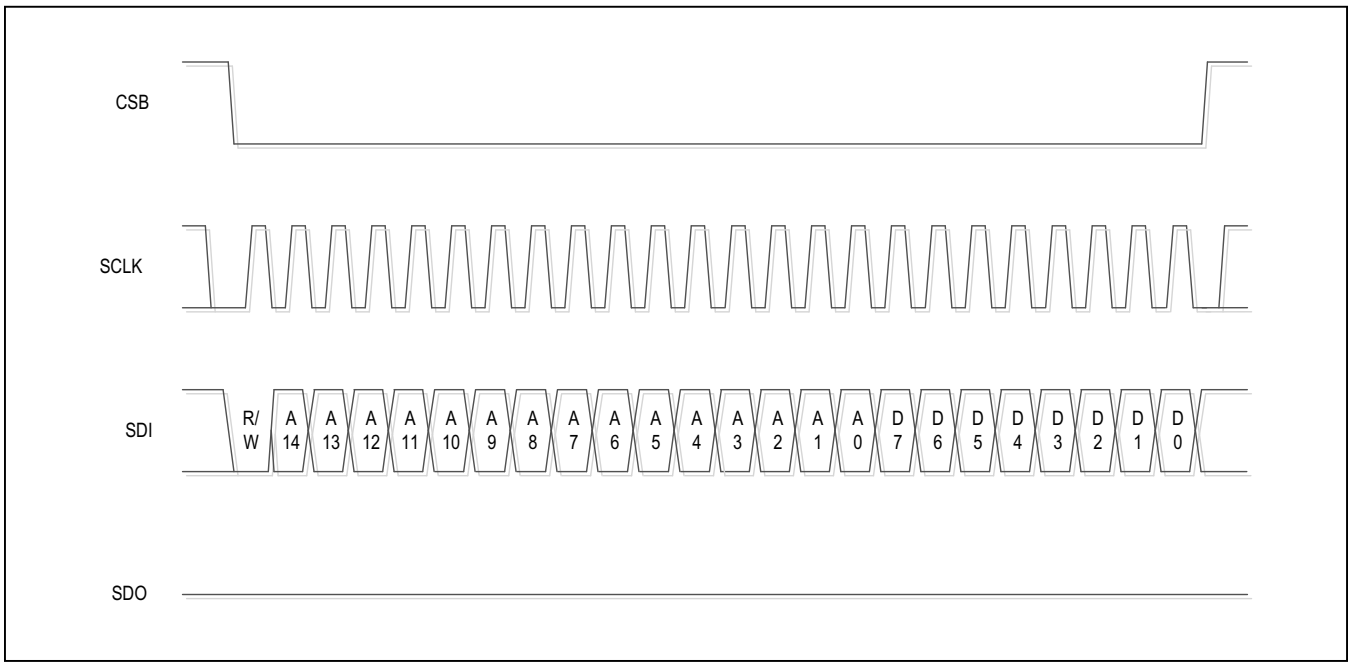


Figure 12. SPI Single Write with MSB-First Format

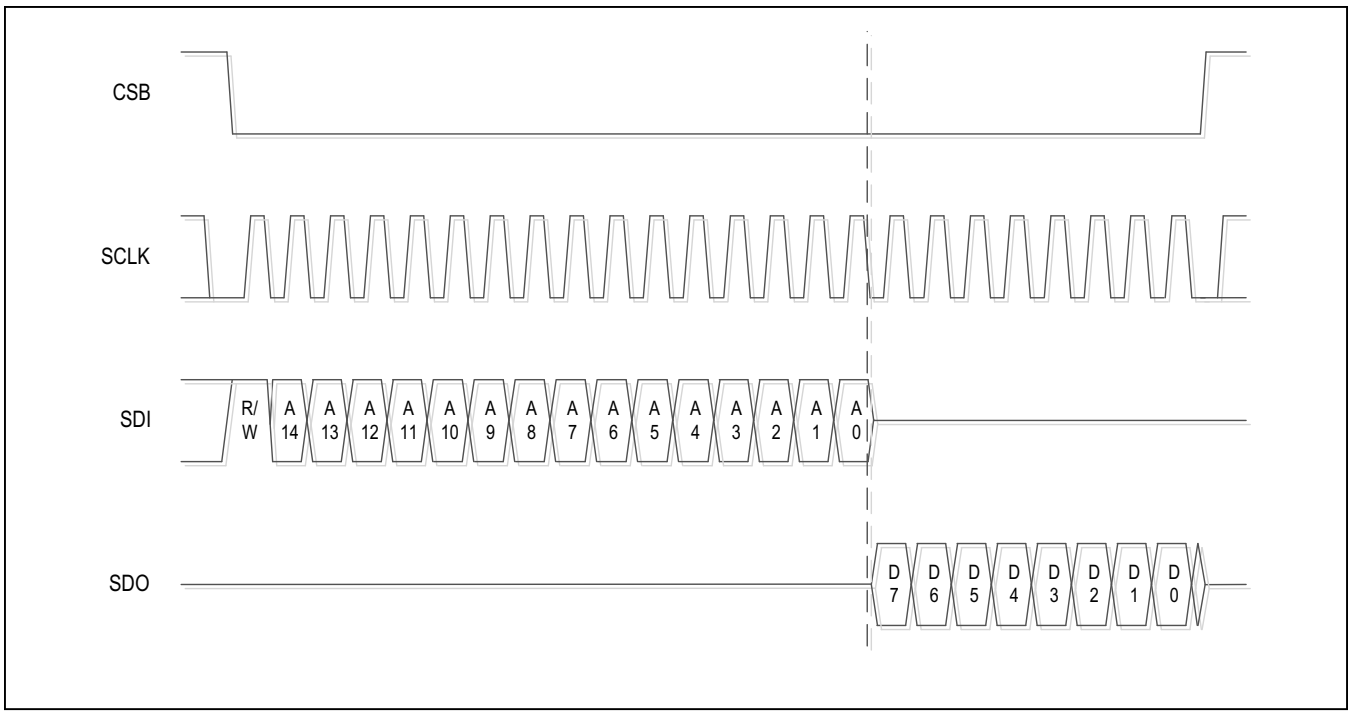


Figure 13. SPI Single Read with MSB-First Format

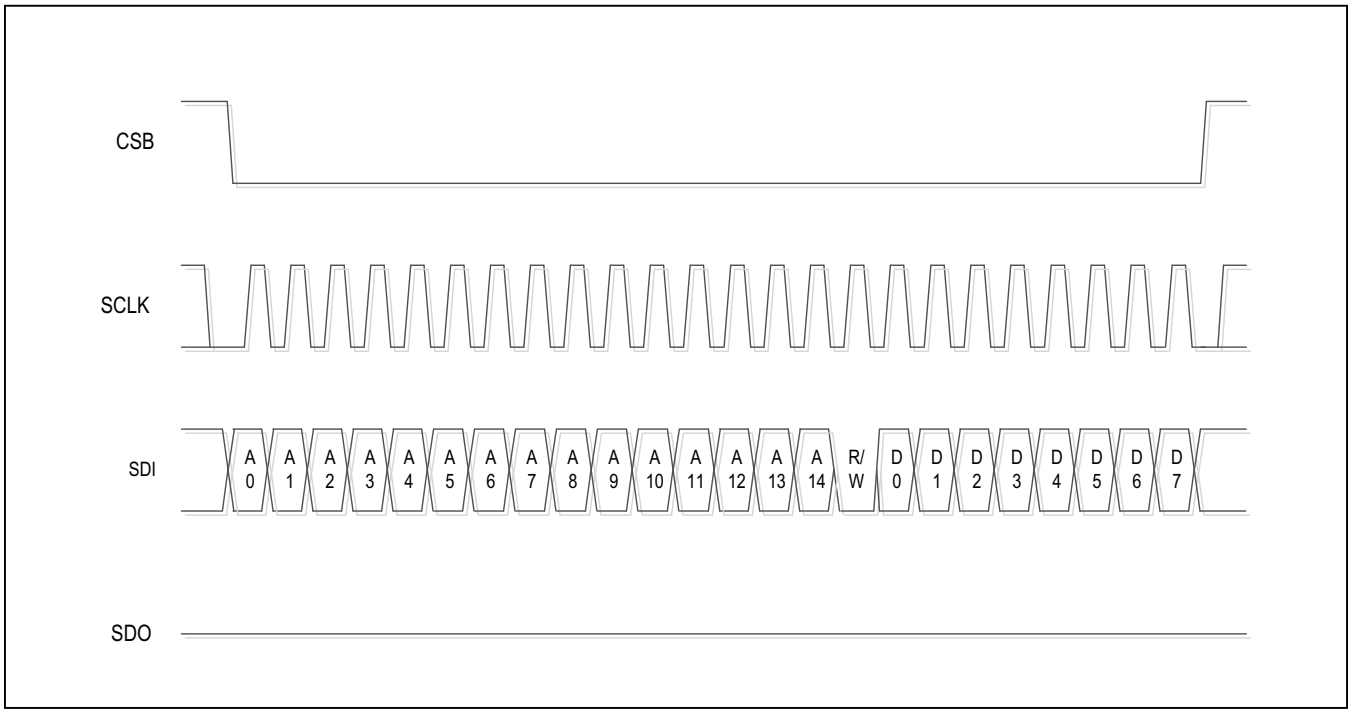


Figure 14. SPI Single Write with LSB-First Format

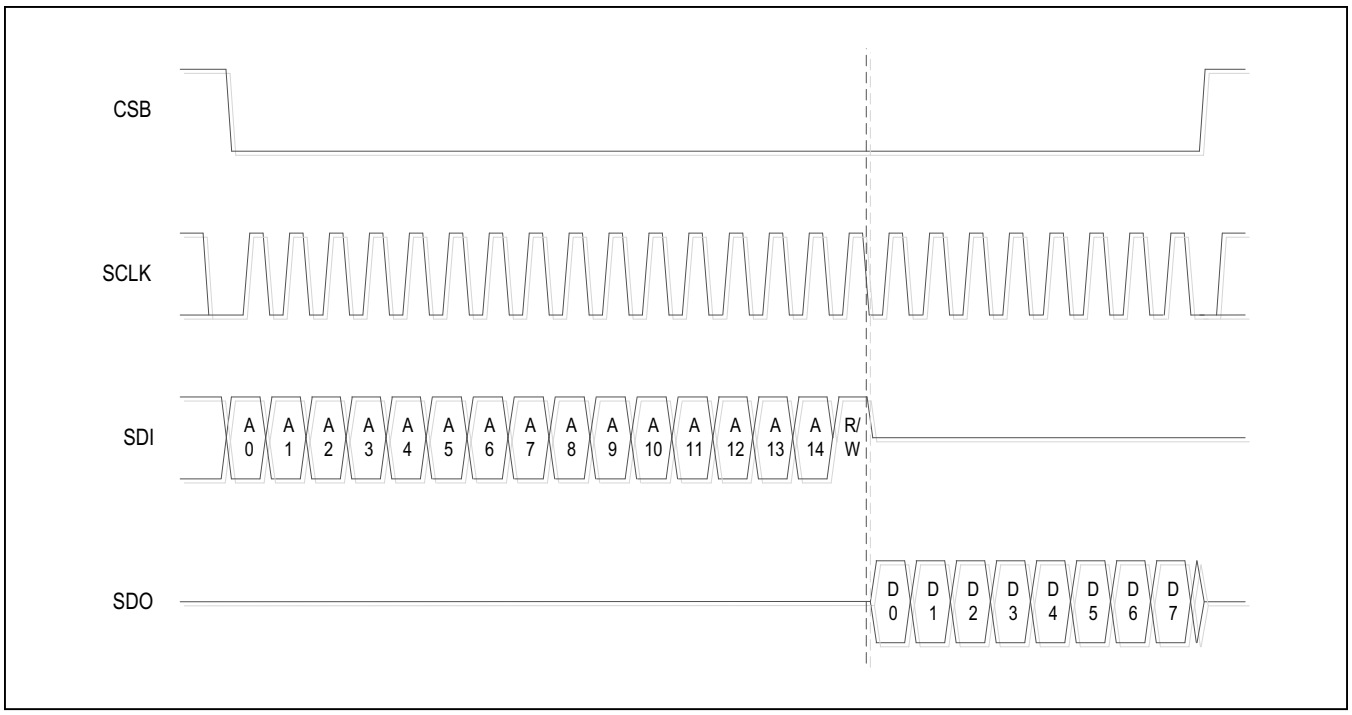


Figure 15. SPI Single Read with LSB-First Format

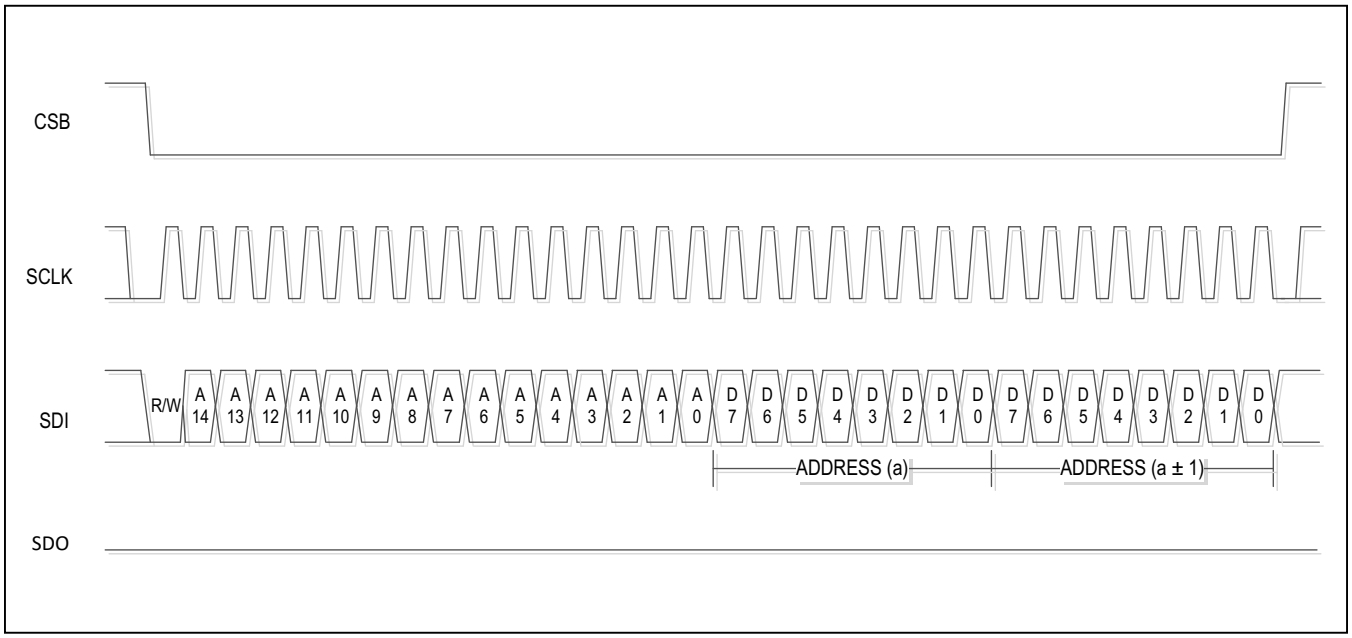


Figure 16. SPI Burst Write with MSB-First Format

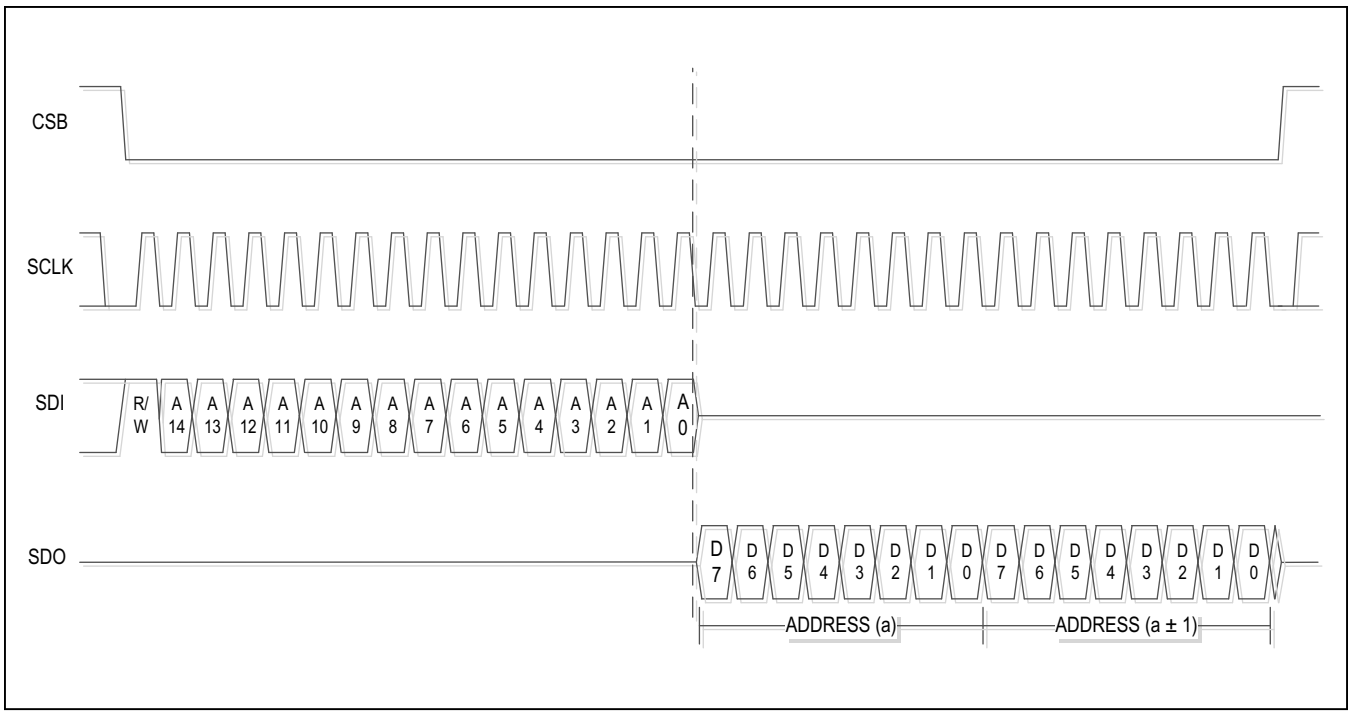


Figure 17. SPI Burst Read with MSB-First Format

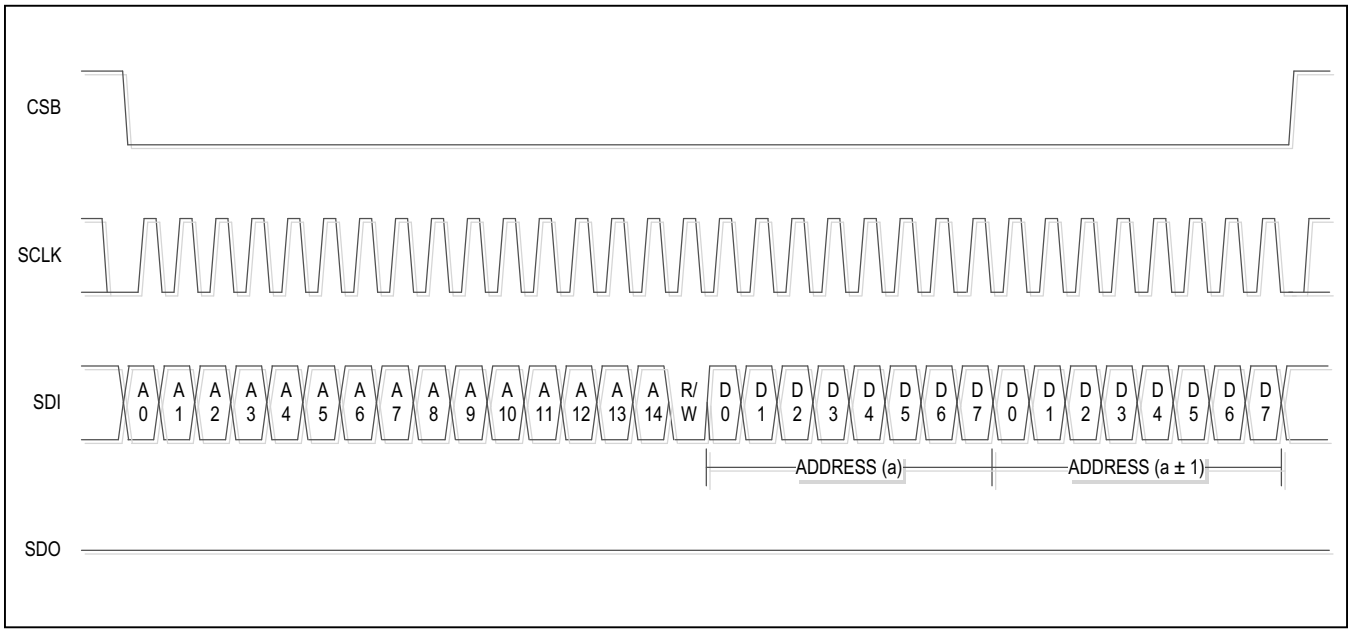


Figure 18. SPI Burst Write with LSB-First Format

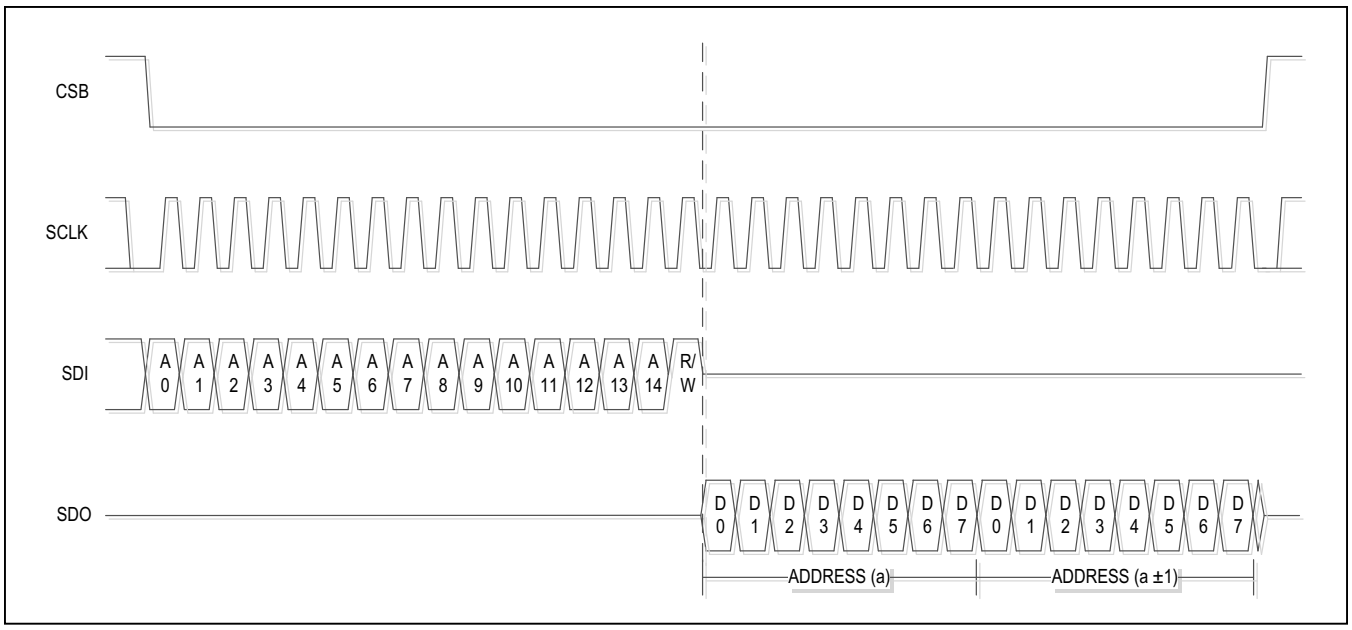


Figure 19. SPI Burst Read with LSB-First Format

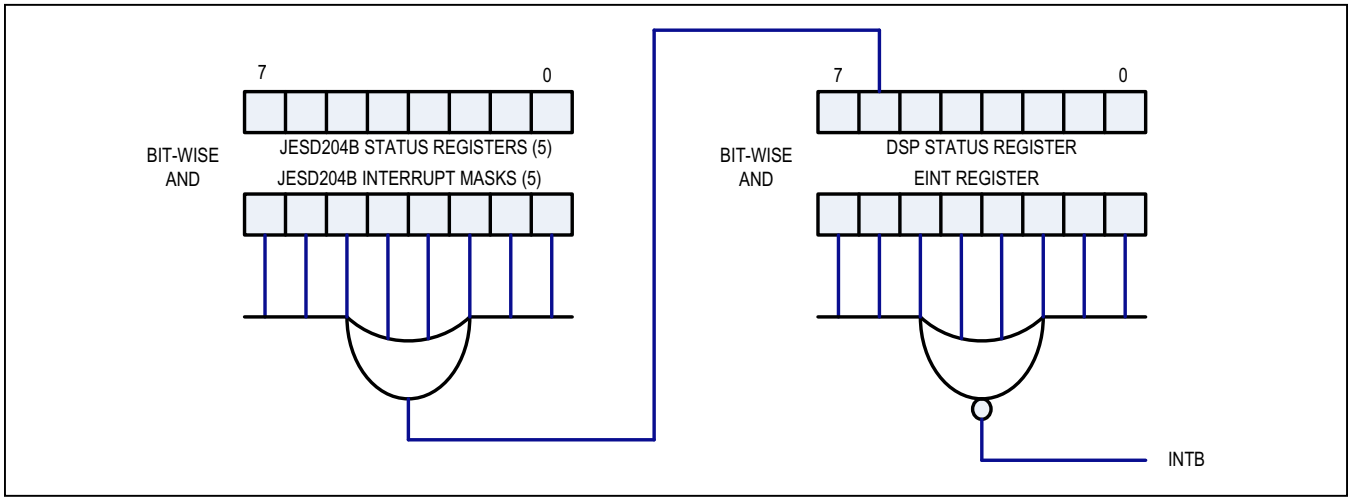


Figure 20. Interrupt Tree

Interrupt Control

The INTB pin is a 1.8V CMOS logic output that signals an interrupt condition when in a low state. The interrupt system is comprised of a status register and an interrupt mask register. The interrupt signal is an 8-input logic NOR of the EINT register bit-wise ANDed with the DSP status register. The interrupt tree for the device is shown in Figure 20. The JESD204B interface has its own second level of interrupt registers and interrupt mask registers as defined in the register map. The interrupt masks and registers can be modified through the serial interface. Table 4 shows all the status register bits that can be enabled to generate an interrupt.

Table 4. Status Register Bits

DSP STATUS REGISTER (1ST LEVEL INTERRUPT)	
BANK.REGISTER.BIT	**Function**
DSP.STATUS.JSDIM	Real-time, DAC mute from JESD LINK Layer is active
DSP.STATUS.JSDII	Real-time, interrupt from JESD LINK Layer is active
DSP.STATUS.TRDY	Latched, internal trim load is complete and the SPI bus is unblocked for external access
DSP.STATUS.PLLIck	Latched, DAC PLL was **unlocked**.
JESD204B Status Registers (2nd Level Interrupt)	
BANK.REGISTER.BIT	**Function**
RLaneRegs0-5.StatRlane.FrNSync	Real-time, Frame synchronization state machine is not synchronized on Lane N
RLaneRegs0-5.StatRlane.LnReAlign	Latched, lane realignment occured on Lane N
RLaneRegs0-5.StatRlane.FrReAlign	Latched, frame realignment occured on Lane N
RLaneRegs0-5.StatRlane.DISP	Latched, Disparity error detected on Lane N
RLaneRegs0-5.StatRlane.NIT	Latched, NIT error detected on Lane N
RLaneRegs0-5.StatRlane.CGS	Latched, Code Group Synchronization state-machine was not synchronized on Lane N
RLaneRegs0-5.StatRlane.FIFOempty	Latched, FIFO empty on Lane N
RLaneRegs0-5.StatRlane.FIFOfull	Latched, FIFO full on Lane N
RLaneRegs0-5.StatRlane.PRBSerr	Latched, PHY interface PRBS monitor detected an error on Lane N
RLaneRegs0-5.StatRlane.KContErr	Latched, non-/K/ character detected on Lane N
RLaneRegs0-5.StatRlane.FChkErr	Latched, ILA sequence FCHK error detected on Lane N
RLaneRegs0-5.StatRlane.LCfgErr	Latched, ILA sequence lane configuration error detected on Lane N
RLaneRegs0-5.StatRlane.ILAerr	Latched, ILA sequence decode (/R/, /Q/, /A/ character) error detected on Lane N
RLinkRegs.StatRlinkILA.ILAnsync	Real-time, ILA synchronization not achieved
RLinkRegs.StatRlinkILA.ILAfailure	Latched, ILA failed, indicates that at least one FIFO in a JESD lane overflowed before the FIFO reads started.
RLinkRegs.StatRlinkPRBS.PRBSerr1	Latched, Converter 2 (Q-sample) PRBS error detected
RLinkRegs.StatRlinkPRBS.PRBSerr0	Latched, Converter 1 (I-sample) PRBS error detected
RLinkRegs.StatRlinkSTP.STPerr1	Latched, Converter 2 (Q-sample) short test pattern error detected
RLinkRegs.StatRlinkSTP.STPerr0	Latched, Converter 1 (I-sample) short test pattern error detected

Digital Control Pins

The MAX5857 contains two 1.8V CMOS logic input control pins: RESETB and MUTE. The device is placed in a reset state when RESETB is logic-low. On power-up, RESETB should remain low until all supply voltages have stabilized and an external clock is applied to CLKP/CLKN. The MUTE pin and the register-based MUTE control when the device enters the mute mode. In mute mode, the DAC digital input is set to mid-scale. A logic-high on the MUTE pin will place the device into mute mode while a logic-low may allow normal operation. The main purpose of MUTE pin is to eliminate any transmit power during the receive time of a TDMA system while the purpose of the MUTE bit is to protect the system PA during startup or error conditions. The register-based mute can be configured through the serial interface enabling the mute mode internally, regardless of the state of the MUTE pin. Similar to the interrupt mask registers, there are mute enable registers which generate the internal mute signal under defined conditions. Table 4 shows all the status register bits that can be used to generate the internal mute. The states of all registers in the device are preserved while the RF DAC output is muted.

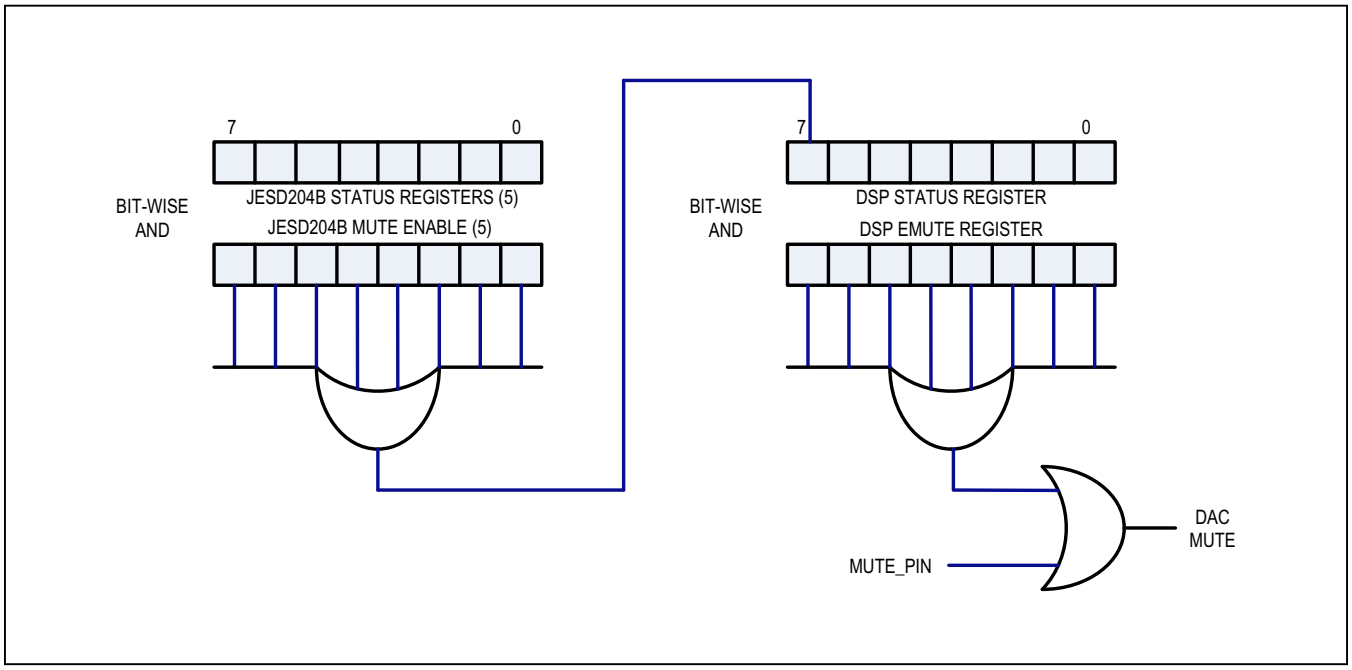


Figure 21. Mute Generation Logic

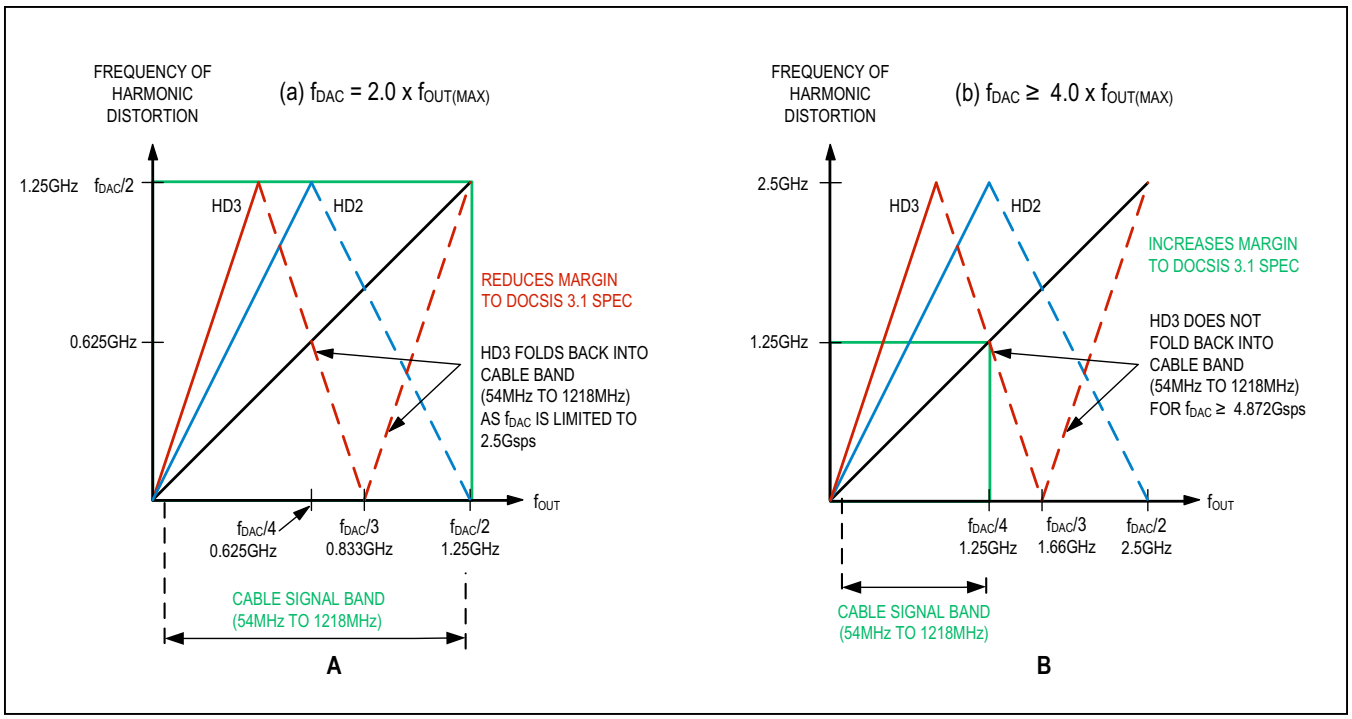


Figure 22. Effect of DAC Update Rate on Folded HD2 and HD3

Frequency Planning

Using a DAC to generate RF transmission signals requires consideration of aliased harmonics and internally generated divided clocks. To ensure the dominant second (HD2) and third order (HD3) harmonics do not fold back into the signal band, the DAC update rate needs to be greater than four times the highest frequency in the band of interest.

Figure 22 A and B show the location of the 2nd and 3rd harmonic distortion products for the case of the DAC being updated at 2 times and 4 times the maximum desired frequency in the band of interest (DOCSIS 3.1 example shown).

Quadrature Modulator and NCO

The device includes a quadrature modulator (Figure 23) that produces an image rejected Real output of the Complex input I-data and Q-data, utilizing a complex numerically controlled oscillator (NCO).

The complex NCO employs a 33-bit phase accumulator to provide a RF signal frequency programmable from DC (0Hz) up to $f_{DAC}/2$. The user needs to calculate and program the following three parameters for proper configuration of the NCO: the Frequency Control Word (FCW), the Numerator Frequency Word (NFW), and the Denominator Frequency Word (DFW).

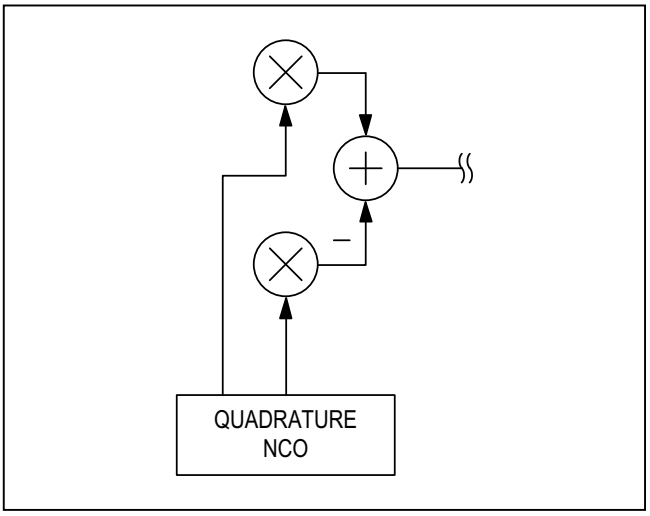


Figure 23. Complex NCO and Modulator

$$FCW_{full} = \frac{2^{33} \cdot f_{NCO}}{f_{DAC}} \quad (1)$$

Where FCW_{full} is the real, floating point, or integer + fractional value of the Frequency Control Word, f_{DAC} is the DAC Sample Rate and f_{NCO} is the target output center frequency of the NCO.

The full FCW is made up of the characteristic or Integer part of the quotient and the fractional remainder or mantissa portion of FCW_{full}:

$$FCW_{full} = FCW + \frac{NFW}{DFW} \quad (2)$$

Where FCW is represented by a 32-bit word, NFW is the Numerator Frequency Word represented by an 18-bit word and the DFW is the Denominator Frequency Word represented with a 19-bit word.

The characteristic or integer part of FCW_{full} is the NCO's primary Frequency Control Word. The remainder or mantissa of the FCW_{full} quotient is converted into two rational integer numbers by removing the common integer multiplication factor. This can be accomplished through brute-force means to find a numerator less than the decimal value of 262144 (2^{18} – 1 or smaller) and a denominator less than 524288 (2^{19} – 1 or smaller). The easiest way to calculate this fraction would be to round the decimal remainder to 5 digits and divide by 100,000. Simplifying the fraction will result in valid programmable values for NFW and DFW.

$$FCW = int\left(FCW_{full}\right) \quad (3)$$

$$\frac{NFW}{DFW} = rem\left(FCW_{full}\right) \quad (4)$$

When setting DFW to 100,000 and rounding the decimal remainder to 5 digits the mantissa can be accurately represented as a ratio of two numbers: NFW and DFW.

To determine the programming precision of the NCO based on the least significant bit (LSB) size of the NCO, use the following equation:

$$FCW_{1Hz} = \frac{2^{33}}{f_{DAC}} \quad (5)$$

Where FCW_{1Hz} is the LSBs required (whole and fractional) to adjust the NCO frequency by a 1Hz step.

$$f_{NCO/LSB} = \frac{1}{FCW_{1Hz}} = \frac{f_{DAC}}{2^{33}} \quad (6)$$

Where $f_{NCO/LSB}$ is the frequency change to the NCO (f_{NCO}) given a single, whole LSB step of the NCO control word.

This $f_{NCO/LSB}$ value essentially shows the precision of the NCO with the largest step size being about 0.7Hz per LSB change in the NCO control word. Using the fractional portion of the FCW will result in precision adjustments as small as 2.7µHz.

Example 1

Use the following system values to calculate the FCW, NFW, and DFW:

f_{DAC} = 5898.24MHz, and f_{NCO} = 575MHz

Starting with equation (1):

$$FCW_{full} = \frac{2^{33} \cdot f_{NCO}}{f_{DAC}} = \frac{2^{33} \cdot 575M}{5898.24M}$$

$$FCW_{full} = 83740444.\overline{4}...$$

Using equations (3) and (4):

$$FCW = int(837404444.44444) = 837404444$$

$$\frac{NFW}{DFW} = rem\left(837404444.44444\right) = 0.44444$$

$$\frac{NFW}{DFW} = \frac{44444}{100000} = \frac{11111}{25000} \approx \frac{112}{252}$$

$$NFW = 112, \quad DFW = 252$$

Equation (1) can be used in reverse to find an NCO frequency based off of an integer multiple of FCW (where the fractional portion does not require programming):

$$f_{NCO} = \frac{f_{DAC} \cdot FCW}{2^{33}} = \frac{5898.24M \cdot 837404444}{2^{33}}$$

$$f_{NCO} = 574.999999695MHz$$

The above result confirms that the target NCO frequency is produced to a sub-1Hz precision.

Calculating the $f_{NCO/LSB}$ using equation (6):

$$f_{NCO/LSB} = \frac{f_{DAC}}{2^{33}} = \frac{5898.24M}{2^{33}} = 0.68665Hz/LSB$$

Thus, without using the fractional NCO words, the NCO can be adjusted to a resolution of better than 0.7Hz and

in this example, set to a precise value within 0.305Hz of the target frequency.

Example 2

Use the following system values:

f_{DAC} = 4915.20MHz, and f_{NCO} = 573MHz

Using equation (1):

$$FCW_{full} = \frac{2^{33} \cdot f_{NCO}}{f_{DAC}} = \frac{2^{33} \cdot 573M}{4915.20M}$$

$$FCW_{full} = 1001390080.00000$$

Using equations (3) and (4):

$$FCW = int(100390080.00000) = 1001390080$$

$$\frac{NFW}{DFW} = rem\left(1001390080.00000\right) = 0.00000$$

$$NFW = 0, \quad DFW = 0$$

The following is example Matlab code for calculating NCO values. When calculating FCW, NFW, and DFW, use long format types for more precise results.

```
% Find out MAX5857 NCO values
format long
% Define DAC clock frequency
Fdac = 5859.24e6*M
% Define desired NCO frequency
Fnco = 1796.769375e6;
FCW_full = 2^33*Fnco/Fdac;
% Calculate FCW, NFW and DFW
FCW = floor(FCW_full)
rats(FCW_full-FCW)
% END
```

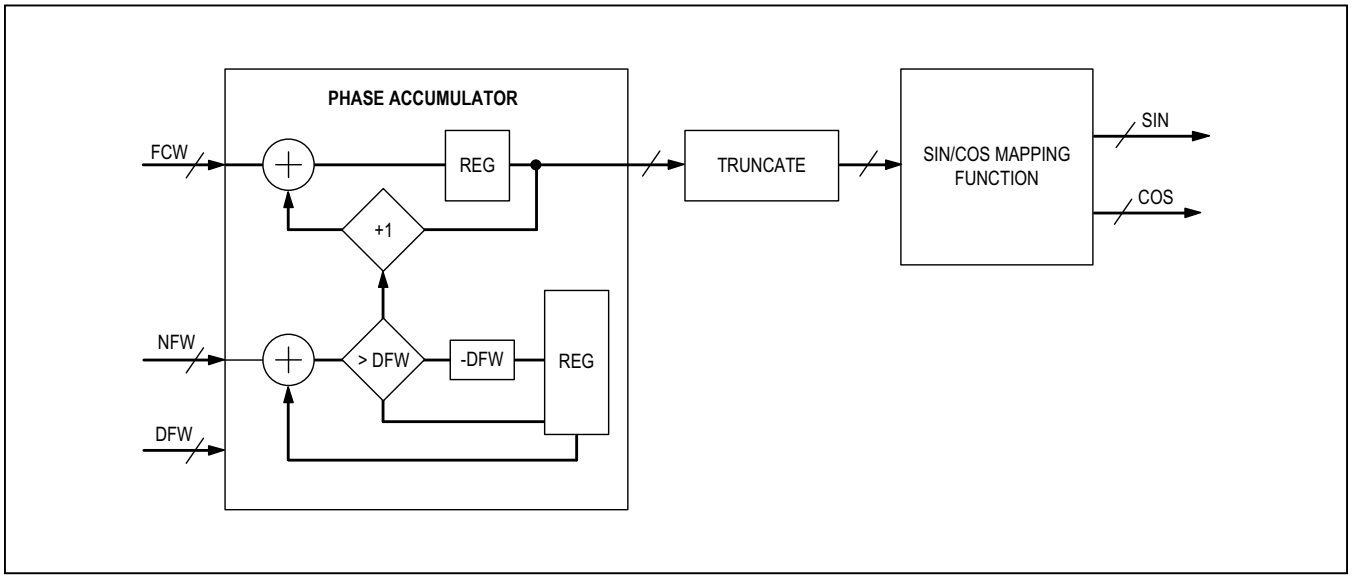


Figure 24. NCO Block Diagram

Analog Interface

Reference Interface

The device operates with either the on-chip 1.2V bandgap reference or an external reference voltage source as shown in Figures 25 A and B. REFIO serves as the input for an external, low-impedance reference source, or as the reference output when the internal reference is used. REFIO must be decoupled to DACREF with a 1µF capacitor when using the internal reference. REFIO must be buffered with an external amplifier if heavier loading is required, due to the 10kΩ series resistance.

The reference circuit employs a control amplifier designed to regulate the full-scale, differential output current, I_{OUTFS}. The output current is calculated as follows:

$$I_{OUTFS} = 32 \cdot I_{REF} \quad (7)$$

$$I_{REF} = \frac{V_{REFIO}}{R_{SET}} \quad (8)$$

Where I_{REF} is the reference output current and I_{OUTFS} is the full-scale output current of the DAC.

In general, the dynamic performance of the DAC improves with increasing full-scale current. Using the 1.2V (typical) internal reference and R_{SET} of 965Ω results in the maximum full-scale output current of 40mA.

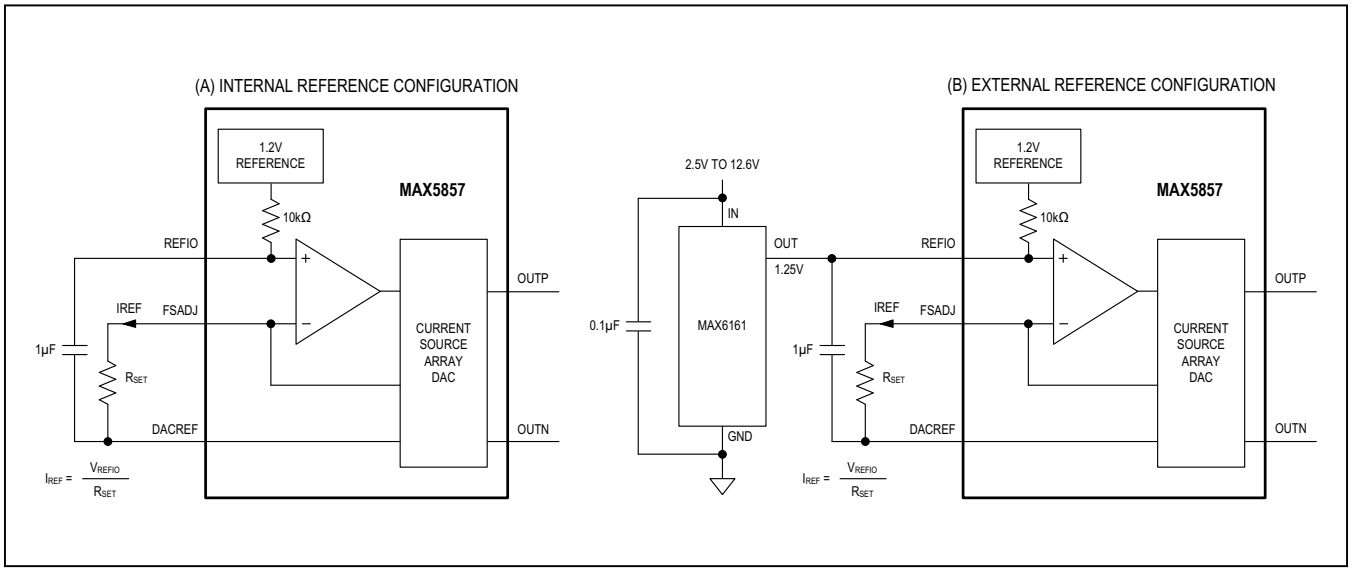


Figure 25. Setting the DAC Output Full-Scale Using an Internal (A) or External Reference Voltage (B)

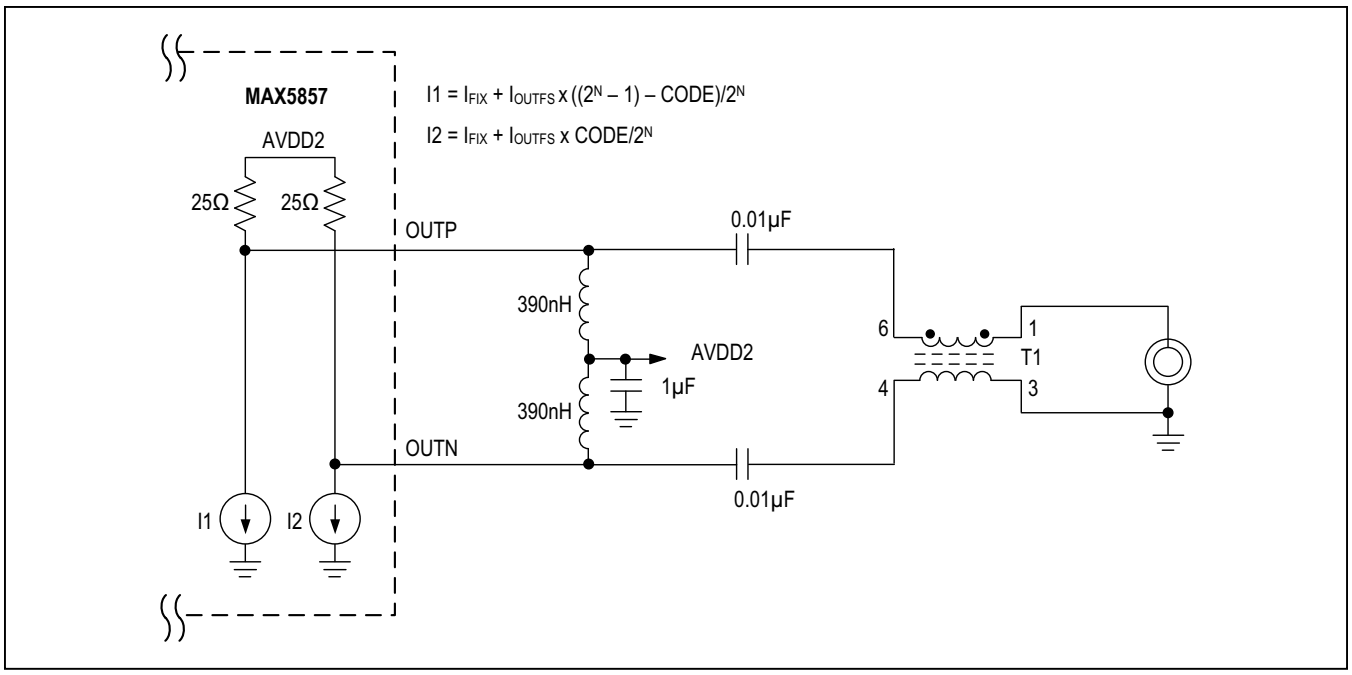


Figure 26. Typical DAC Output Configuration

Analog Output

The device is a differential current-steering DAC with built-in output termination resistors. The outputs are terminated to AVDD2 providing a 50Ω differential output resistance. In addition to the signal current, a constant current sink (I_{FIX}) equal to one half I_{OUTFS} is connected to each differential DAC output. Figure 26 shows an equivalent circuit for the internal output structure of the device. The circuit has some resistive, capacitive and inductive elements. These elements have been minimized in order to achieve the highest possible output bandwidth (2.6GHz, typical).

In addition, the device requires a differential external termination (i.e., double termination). This external termination can be accomplished with a differential 50Ω load or a single-ended 50Ω load interfaced through a transformer. RF chokes to the AVDD2 supply should be used with the transformer coupled output. A typical transformer coupled configuration for high-frequency operation is shown in Figure 26.

For applications where the DC information is important, the output configuration in Figure 27 can be used. 25Ω resistors to AVDD2 are required for DC coupling. The DC configuration will lower the output common-mode voltage which may reduce performance slightly. The output termination along with the full-scale current must maintain a voltage swing within the Output Compliance range of the device (as specified in the *Electrical Characteristics* table).

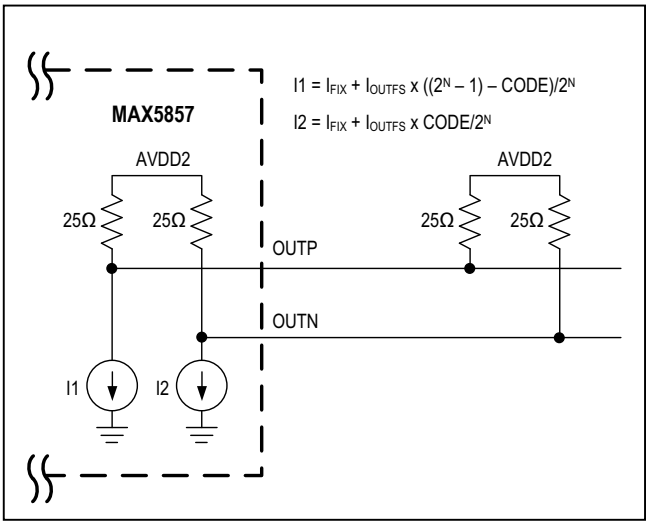


Figure 27. Output Configuration for Low Frequency Operation

Clock Interface

The DAC contains a differential high-frequency clock input, CLKP/CLKN, and an optional (bypassable) internal clock multiplying PLL to ease clock distribution. When the PLL is bypassed, the DAC is updated on the rising edge of CLKP/CLKN at maximum frequency of 5898.24MHz. See the *DAC Clock PLL* section for operation with PLL enabled.

The high-frequency clock should be a balanced, fully differential signal with a 50%, or near-50% duty cycle. The clock input has internal (on-chip) 100Ω differential termination. The clock requires a minimum input power of 0dBm. The clock inputs must be AC-coupled to the source as they are internally self-biased.

Clock Subsystem

Overview

The MAX5857 clock subsystem is outlined in Figure 28. The differential DAC input clock CLKP/N is received through a differential clock interface buffer.

From the clock buffer output the clock can either be routed directly to the DAC core or it can be used as a reference clock for an on-chip DAC PLL.

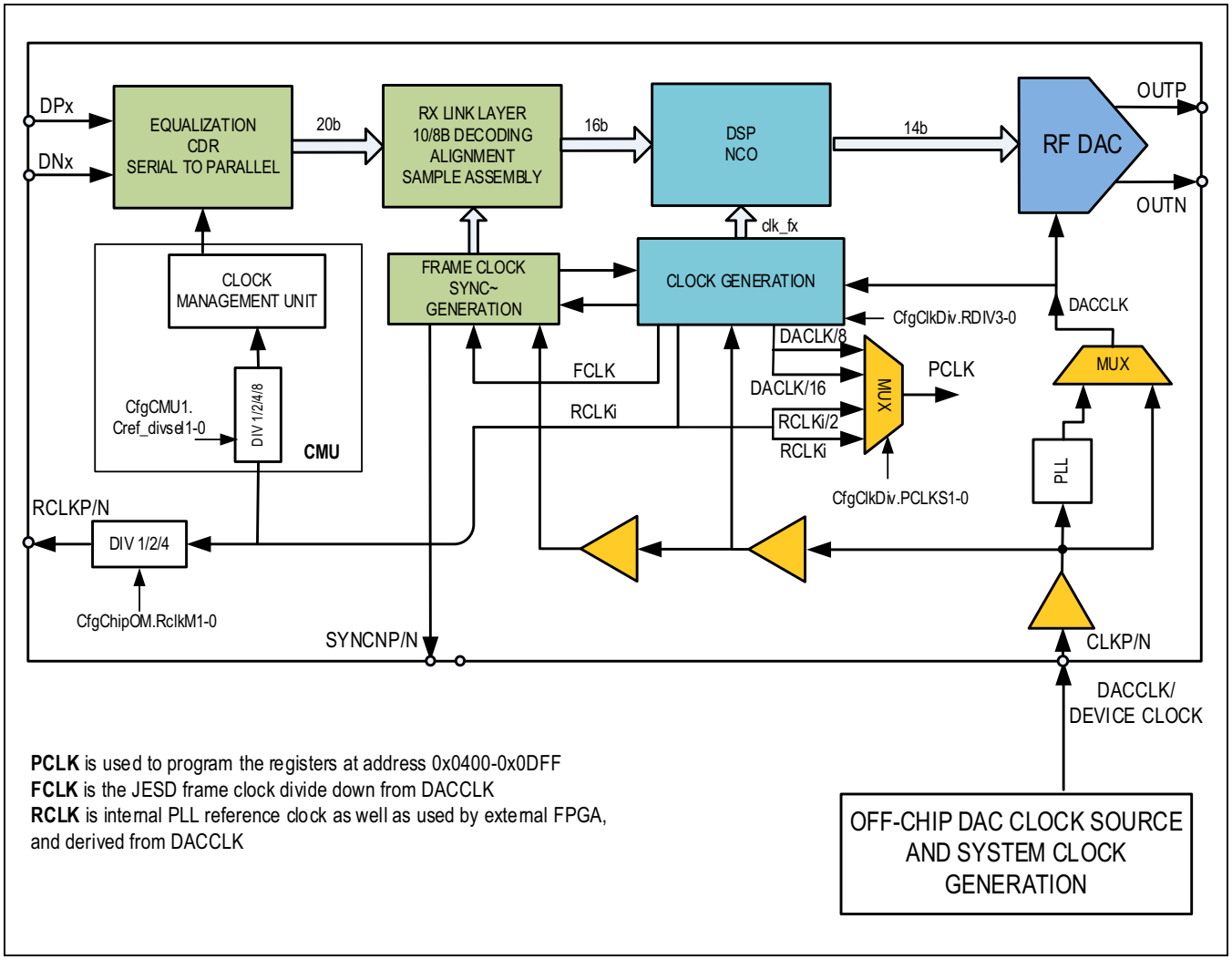


Figure 28. MAX5857 Clock Subsystem

If the PLL is bypassed, the input clock frequency is equal to the DAC update rate, which can be up to 5.9GHz. In this mode, the only restriction on the DAC clock frequency is that it results in a supported serial interface data rate with a valid number of active JESD204B lanes.

The PLL should be bypassed if the application requires best possible phase noise and wide-band jitter performance. In that case using a high quality off-chip clock source will allow for highest achievable DAC phase noise and jitter performance. For the DAC clock quality requirements refer to the *Clock Requirement* section of this document.

If the PLL is enabled, the DAC input clock is used as a PLL reference clock and its frequency is multiplied by a programmable constant. In that case the input DAC clock frequency can be much lower than the DAC update rate. However, the DAC output signal phase noise and jitter will be mostly determined by the on-chip PLL performance. The reference clock phase noise will be dominant within the 100kHz PLL loop bandwidth. In that frequency range the input clock phase noise will be amplified by 20 x $\log(F_{DAC}/F_{REF})$.

DAC Clock PLL

The MAX5857 differential high-frequency clock input (CLKP/CLKN) accepts an external reference clock signal that can be multiplied internally by a phase-locked-loop (PLL). The PLL includes user-programmable multiplication factors which provide flexibility in the reference clock selection. Figure 29 shows the functional block diagram of the PLL.

The reference input signal is divided by 1, 2, 4, or 8 under user control before being applied to the phase/frequency detector (PFD). The VCO output is divided by a programmable divide-by 16, 20, 24, or 28 before it is fed back to the PFD. In addition to the programmable reference divider and programmable VCO divider, there is an optional output divide by 2, before the clock signal is supplied to the RF DAC.

Table 5 summarizes frequency multiplication factors between an external reference clock and DACCLK for various PLL settings.

Table 5. PLL Configuration Settings and Overall Clock Frequency Multiplier

REFERENCE DIVIDER	FEED-BACK DIVIDER	VCO MULTIPLIER	POST DIVIDER	OVERALL FREQUENCY MULTIPLIER
2	16	8	1	8
2	20	10	1	10
2	24	12	1	12
2	28	14	1	14
2	16	8	2	4
2	20	10	2	5
2	24	12	2	6
2	28	14	2	7
4	16	4	1	4
4	20	5	1	5
4	24	6	1	6
4	28	7	1	7
4	16	4	2	2
4	20	5	2	2.5
4	24	6	2	3
4	28	7	2	3.5
8	16	2	1	2
8	20	2.5	1	2.5
8	24	3.0	1	3
8	28	3.5	1	3.5
8	16	2	2	1
8	20	2.5	2	1.25
8	24	3.0	2	1.50
8	28	3.5	2	1.75

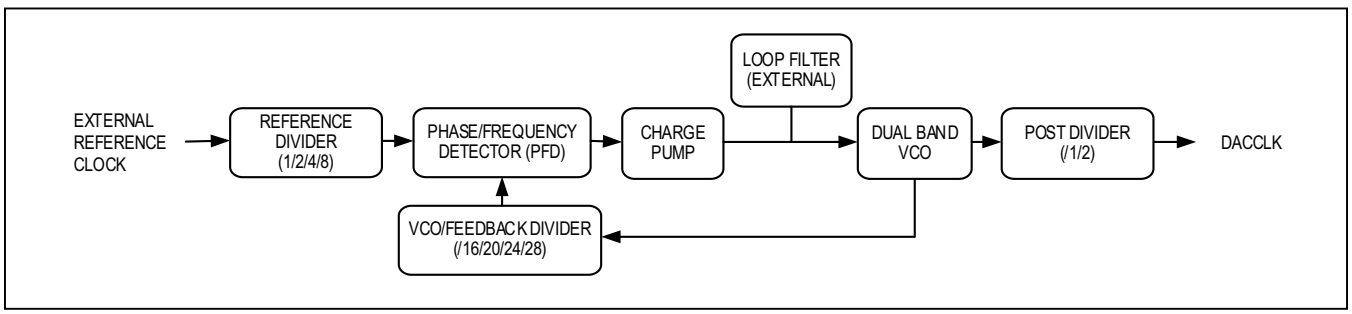


Figure 29. DAC Clock PLL Functional Block Diagram

VCO Band Select

The VCO has two frequency ranges. The low range supports 4.42368GHz and 4.9152GHz operation and the high range supports 5.89824GHz. The combination of reference frequency, reference divide and feedback divide values, and VCO band select must be chosen to operate the VCO within one of its allowed frequency ranges.

Lock Detect

The DAC clock PLL includes a lock detect indicator which can be read out of the SPI status register (DSP.StatPLL0). Bit PLL_LOCK is set high when the PLL is locked and low when the PLL is unlocked.

PLL External Components

The DAC clock PLL requires external loop filter components. Figure 30 shows the schematic for the loop filter. The loop filter components should be placed as close as possible to the MAX5857 to avoid noise coupling into the circuit.

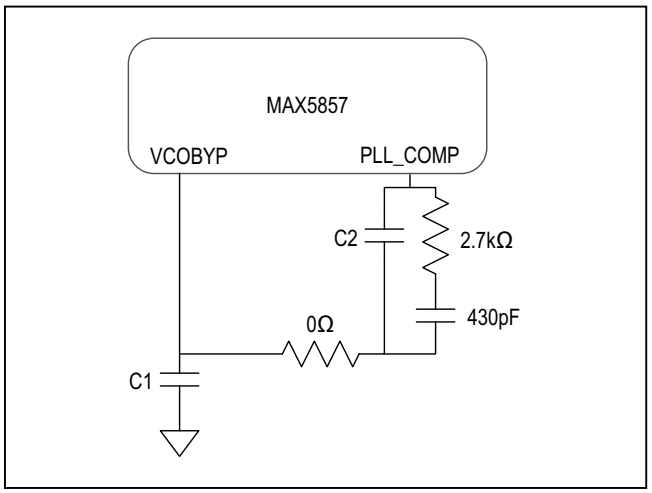


Figure 30. DAC Clock PLL External Components

In addition to the loop filter, there is a bypass capacitor that must be placed very close to the MAX5857. The C1 nF and C2 pF capacitor values strongly depends on system PCB design and are unique for most designs (see *Applications Guidelines*).

The user may wish to select different operating conditions for the PLL loop filter than those specified. The following values may be useful for calculating new compensation component values:

VCO Gain: K_{VCO} = 115MHz/V

Charge Pump Current: I_{CP} = 480µA

PLL Feedback Divider Setting: N = <CfgPLL2.DVAL[3:2] and CfgPLL1.DVAL[1:0]>

Internal Smoothing Capacitance: C_S = 43pF

RCLK Description and Use

The MAX5857 outputs a divided reference clock RCLK (RCLKP/RCLKN) that is equal to the DAC clock frequency divided by a factor (Defined by programming the register bits DSP.CfgClkDiv.RDIV) to ensure synchronization with the system clock. Caution must be exercised when programming the DSP.CfgClkDiv.RDIV register due to its performance impact on other internal blocks. Refer to the *Frequency Settings and Configuration* section for more details.

The output clock RCLKP/RCLKN frequency can be further lowered by programming the control bits in the DSP.CfgChipOM.RclkM register.

Interpolation Filters

The MAX5857 has powerful digital signal process capability with its built-in digital interpolation filters with an interpolation ratio of 4x (complex path). Table 6 shows the digital filter coefficients of 4x (F1, F2 cascaded) interpolation ratios.

Table 6. Digital Filter Coefficients

TAP	F1 2X (COMPLEX PATH)	F2 2X (COMPLEX PATH)
1	0.00004577636718750	0.00138854980468750
2, 4, 6, 8, 12, 14, 16, 18	0	0
3	-0.00015258789062500	-0.01086425781250000
5	0.00039672851562500	0.04589843750000000
7	-0.00083923339843750	-0.14880371093750000
9	0.00161743164062500	0.61239624023437500
10	0	1
11	-0.00286865234375000	0.61239624023437500

Table 6. Digital Filter Coefficients (continued)

TAP	F1 2X (COMPLEX PATH)	F2 2X (COMPLEX PATH)
13	0.00479125976562500	-0.14880371093750000
15	-0.00762939453125000	0.04589843750000000
17	0.01168060302734380	-0.01086425781250000
19	-0.01736450195312500	0.00138854980468750
20, 22, 24, 26, 28, 30, 32, 36, 38, 40, 42, 44 46, 48, 50, 52, 54, 56, 58, 60, 62, 64, 66	0	
21	0.02522850036621090	
23	-0.03616333007812500	
25	0.05177307128906250	
27	-0.07537841796875000	
29	0.11575317382812500	
31	-0.20507812500000000	
33	0.63421630859375000	
34	1	
35	0.63421630859375000	
37	-0.20507812500000000	
39	0.11575317382812500	
41	-0.07537841796875000	
43	0.05177307128906250	
45	-0.03616333007812500	
47	0.02522850036621090	
49	-0.01736450195312500	
51	0.01168060302734380	
53	-0.00762939453125000	
55	0.00479125976562500	
57	-0.00286865234375000	
59	0.00161743164062500	
61	-0.00083923339843750	
63	0.00039672851562500	
65	-0.00015258789062500	
67	0.00004577636718750	

Register Definition and Description

The detailed description about the configuration registers in the MAX5857 can be found in the section *Register Map*, which can be configured through SPI serial control interface.

SPI to PCLK Frequency Ratio

The MAX5857 use a internally generated clock (PCLK) for the configuration of registers with the address between 0x0400 and 0x0DFF (RLinkRegs, RLaneRegs0-5, SerDesRegs, CMURegs, PHY0-5 register banks). PCLK is simply a divided down version of the internal DAC clock (DACCLK), and varies in proportion to that frequency. PCLK has the minimum and maximum frequency range required for the proper operation of the device.

- PCLK must be at least 14 times faster than the SPI clock
- PCLK frequency cannot be greater than 300MHz.

This clock period relation is not required if the user is accessing any register below the 0x0400 address range (GLBL and DSP banks). The PCLK frequency can be selected using the control bits DSP.CfgClkDiv.PCLK, as per Table 7. This configuration must be performed before accessing any register between addresses 0x0400 and 0x0DFF.

Table 7. PCLK Frequency Selection

PCLK CONTROL BITS	SOURCE FOR PCLK
00*	RCLK div 2
01	RCLK
10	DACCLK div 16
11	DACCLK div 8

**Default Setting*

PCLK Control Bits are set in the DSP.CfgClkDiv.PCLK register

To select RCLK, write the appropriate division factor noted in the DSP.CfgClkDiv.RDIV register description. For a DAC frequency of 4915.2MHz, the default setting will results in a PCLK of 4915.2/24 = 204.8MHz (default setting of RCLK is DACCLK/12, and PCLK = RCLK/2).

Auto Selection of PCLK

The MAX5857 will internally update the DSP.CfgClkDiv register (RDIV and PCLKS bits) to select the appropriate PCLK output frequency whenever the GLBL.CfgDACrate or RLinkRegs.CfgRLinkParam1.CfgL register values are updated. These register settings will automatically configure the RDIV (RCLK divide ratio) and PCLKS (PCLK Source) value as per Table 8. Internal configuration of the DSP.CfgClkDiv register is also based on the DAC clock frequency listed in Table 8. If any other clock settings are required, the user can manually program the DSP.CfgClkDiv register.

Table 8. RCLK and PCLK Auto Configuration Example

JESD LANES	DAC UPDATE RATE	DACCLK FREQUENCY (MHZ)	RDIV	RCLK FREQUENCY (MHZ)	PCLKS	PCLK FREQUENCY (MHZ)
6	6	5898.24	6	491.52	0	245.76
6	4	4423.68	6	368.64	2	276.48
6	2	3686.4	6	307.2	2	230.4
6,3	1	2949.12	6	245.76	1	245.76
5	5	4915.2	8	245.76	1	245.76
5	0	2457.6	8	122.88	3	307.2
4	3	3932.16	4	491.52	2	245.76
4	0	2457.6	4	307.2	1	307.2
4	1	2949.12	4	368.64	2	184.32

DAC Update Rate enumerated register value at address 0x10

RDIV is the RCLK Divide Ratio at address 0x185

PCLKS is the PCLK Source at address 0x185

SPI to f_{DAC} Frequency Ratio

The DAC clock is used to derive internal functional clocks, and these divided-down clocks interact with the SPI clock (SCLK) during the register configuration. Therefore the SPI clock frequency selection must follow these guidelines.

- The SCLK frequency cannot exceed 20MHz.
- The SCLK frequency cannot be greater than the DAC update rate divided by 24 ($f_{DAC}/24$).

Note: SPI interface also has hold time requirement for the CSB pin. The hold time between a CSB signal going high to the falling edge of last SCLK is 48 fDAC clock periods. See Figure 1 for other serial interface timing details.

Device Configuration

The device configuration must be performed using a prescribed sequence.

The first step is to configure the SPI interface format. This is done by writing to the SPI register GLBL.CfgIFA at address 0x00. The control bits in this register form a symmetrical word (palindrome) such that the register can be programmed regardless of pre-existing LSB-first or MSB-first operation. After writing to this register, the SPI interface will be ready for further programming.

The clock mode and the PLL must be configured immediately after the SPI interface.

The next step in the device configuration involves setting up the internal clocks while the CLKP/CLKN input is active. Programming and enabling the PLL clock path may result in internal glitches due to the clock path MUX and PLL settling. Therefore, special care must be taken after resetting the device, when changing between PLL-bypass and PLL-on modes. Once the PLL is enabled, the user must wait at least 20ms, allowing the PLL to settled and locked before continuing on to the next configuration step.

The final step in configuring the PLL is to reset the internal clock dividers. The states of the dividers may have been corrupted by clock glitches during the preceding process.

If the device is powered-up close to the low limit of the operating temperature range (cold), the digital PLL tuning may lock into a state which is not optimized for hot operation. To address this issue, it may be necessary to wait until the device self-heats before a restart of the PLL digital tuning is initiated. A 200ms wait cycle is recommended after the part is configured to allow for warm-up if needed.

After the PLL digital tuning has been restarted, it is necessary to wait 20ms for the PLL to settle and lock again prior to resetting the internal clock dividers.

Once these preceding configurations are complete, the user should allow about 1ms for the internal DSP path to clear out before enabling the DAC output (unmute). If this pause is not included, the DAC output may produce spurious signals due to erroneous data flushing through the DSP signal path.

The MAX5857 configuration sequence is shown in the flow chart of Figure 31.

Frequency Settings and Configuration

The 4x interpolation mode is configured by default with a setting of the DSP.CfgDSP.R3-0 register to 0x0000. NCO complex modulation is always enabled with interpolation.

The prescribed DACCLK rates available in 4x interpolation mode are shown in Table 9.

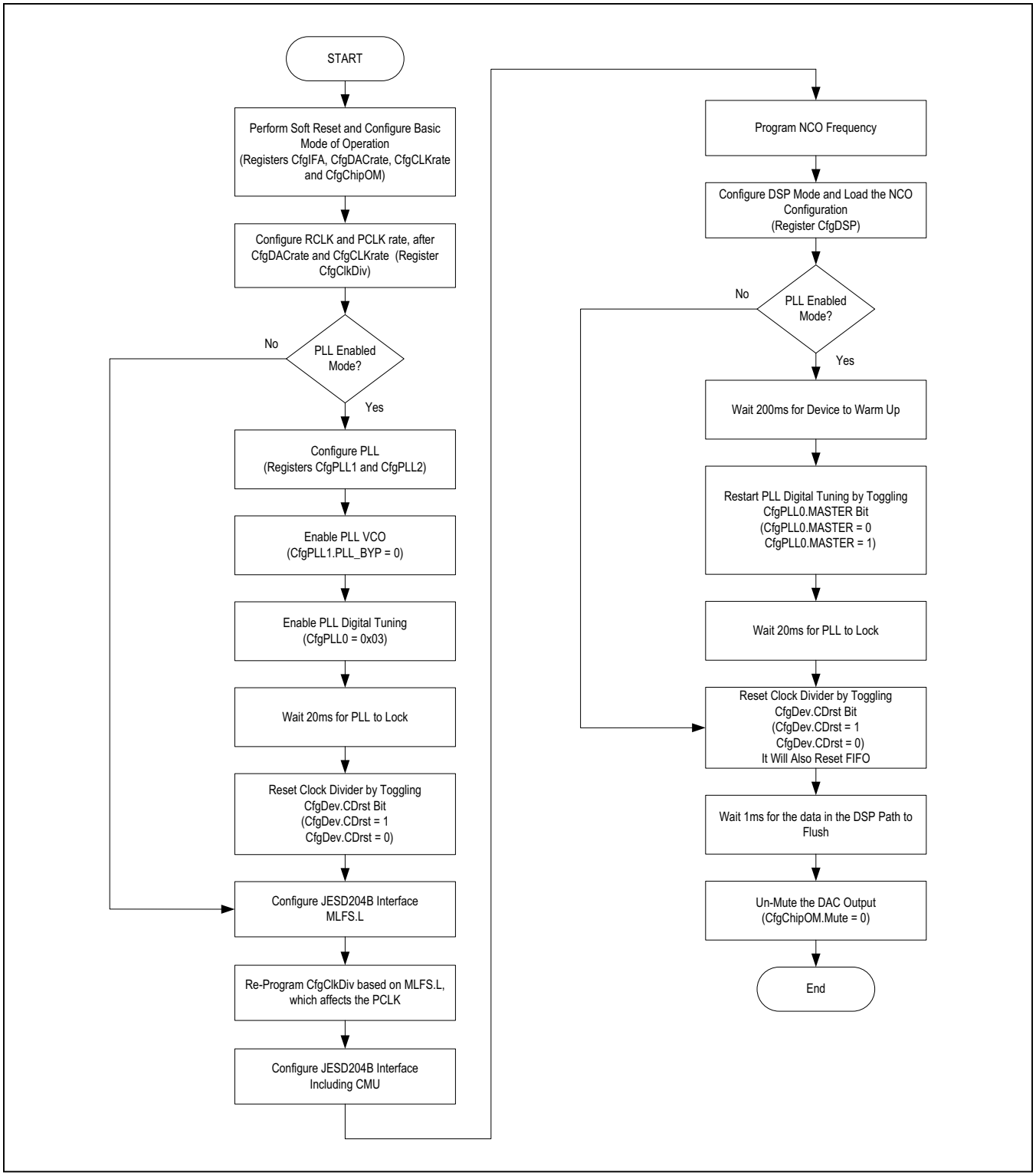


Figure 31. Device Configuration Flow Chart

Table 9. Frequency Planning and Configuration for 4x Mode with CLKP/N Used as JESD204B Device Clock

					FRAME/SAMPLE EXTERNAL						FRAME/SAMPLE DIV DACCLK	
					Frame Rate Div 1		Frame Rate Div 2		Frame Rate Div 4			
DACCLK Frequency (GHz)	Update Rate	JESD Lanes	Sample/ Frame	Lane Rates (GHz)	Input Clock (MHz)	Config Clock Rate	Input Clock (MHz)	Config Clock Rate	Input Clock (MHz)	Config Clock Rate	JESD F-Rate (MHz)	Clock Div F-Rate
5.89824	6	6	3	9.8304	491.52	3	983.04	5	NA	NA	491.52	12
4.91520	5	5	5	9.8304	245.76	0	491.52	3	983.04	5	245.76	20
4.42368	4	6	3	7.3728	368.64	2	737.28	4	NA	NA	368.64	12
2.94912	1	6	3	4.9152	245.76	0	491.52	3	983.04	5	245.76	12
		3		9.8304								
		4	2	7.3728	368.64	2	737.28	4	NA	NA	368.64	8
2.45760	0	5	5	4.9152	NA	NA	245.76	0	491.52	3	122.88	20
		4	2	6.1440	307.20	1	NA	NA	NA	NA	307.20	8

Table 10. Frequency Planning and Configuration for 4x Mode with CLKP/N Not Used as Device Clock

DACCLK FREQUENCY (GHZ)	UPDATE RATE	JESD LANES	SAMPLE/ FRAME	LANE RATES (GHZ)	INPUT CLOCK (MHZ)	JESD F-RATE (MHZ)	CLOCK DIV F-RATE
5.89824	6	6	3	9.8304	5898.24, 2949.12, 1474.56, 983.04, 737.28, 491.52, 368.64, 245.76	491.52	12
4.42368	4	6	3	7.3728	4423.68, 1474.56, 983.04, 737.28, 491.52, 368.64, 245.76	368.64	12
3.93216	3	4	2	9.8304	3932.16	491.52	8
3.6864	2	6	3	6.144	3686.4	307.2	12
2.94912	1	6	3	4.9152	2949.12, 1474.56, 983.04, 737.28, 491.52, 368.64, 245.76	245.76	12
		3		9.8304			
		4	2	7.3728		368.64	8
2.4576	0	4	2	6.144	2457.6, 1228.8, 983.04, 491.52, 307.2, 245.76	307.2	8

NA = Invalid configuration states

Update Rate = Selected DAC update rate multiplier: GLBL.CfgDACrate.Drate

JESD Lanes = Number of JESD Lanes: RLinkRegs. CfgRLinkParam1.CfgL

Sample/Frame = Number of JESD Samples Per Frame: RLinkRegs.CfgRLinkParam1.CfgS

Frame/Sample = Clock source selection from the External Clock or a divided-down version of DACCLK: RLinkRegs.CfgRlinkCtrl.rclk = 0 or 1 respectively. For device clock input less than 1GHz, set to 0. For PLL bypass mode, set to 1 and use the Frame/Sample clock source selection from DAC clock.

Frame Rate Div X JESD Frame Rate divisor 1, 2, or 4 of the Device Clock with RLinkRegs.CfgRlinkSet.DDIV = 0, 1, or 2, respectively

CLKP = External device clock CLKP/CLKN

Config Clock Rate Programmed CLKP configuration value: GLBL.CfgCLKrate.Crate

JESD F-Rate = JESD Frame Rate derived from the DAC update rate.

Clock Div F-Rate = Clock divider setting to generate the JESD Frame Rate: DSP.CfgClkDiv.RDIV

DSP Bypass Function Configuration

Bypassing the interpolation filters and modulator is controlled by configuration bits DSP.CfgDSP.R3-0 in the device. If DSP.CfgDSP.R3-0 is set to 0x0000, the device operates in 4x interpolation mode with modulation enabled. If DSP.CfgDSP.R3-0 is set to 0x0001, the device operates in bypass mode. The maximum DAC rate possible in DSP bypass mode is 2949.12Msps, as shown in Table 11.

Configuration Script Tool

As noted in other sections of this document, proper sequential configuration of the MAX5857 DAC is essential to operating the device as intended. To assist the user with this configuration process, a PERL script tool has been developed which takes ten input parameters and provides an output file containing a sequence of commands that can be written to the device in order to program it for these user-defined operating conditions.

The user provides the input parameters through a text file (with a .txt extension) and the script will generate a sequence of SPI commands and stores them in an output text file (with a .cfg extension). The configuration parameters and the acceptable options used to create the input text file are listed in Table 13.

Table 11. Frequency Planning and Configuration for Bypass Mode with CLKP/N Used as JESD204B Device Clock

					FRAME/SAMPLE EXTERNAL						FRAME/SAMPLE DIV DACCLK	
					Frame Rate Div 1		Frame Rate Div 2		Frame Rate Div 4			
DACCLK Frequency (GHz)	Update Rate	JESD Lanes	Sample/ Frame	Lane Rates (GHz)	Input Clock (MHz)	Config Clock Rate	Input Clock (MHz)	Config Clock Rate	Input Clock (MHz)	Config Clock Rate	JESD F-Rate (MHz)	Clock Div F-Rate
2.94912	1	6	3	9.8304	491.52	3	983.04	5	NA	NA	491.52	6
2.45760	0	5	5	9.8304	245.76	0	491.52	3	983.04	5	245.76	10

Table 12. Frequency Planning and Configuration for Bypass Mode with CLKP/N Not Used as Device Clock

DACCLK FREQUENCY (GHZ)	UPDATE RATE	JESD LANES	SAMPLE/ FRAME	LANE RATES (GHZ)	INPUT CLOCK (MHZ)	JESD F-RATE (MHZ)	CLOCK DIV F-RATE
2.94912	1	6	3	9.8304	2949.12, 1474.56, 983.04, 737.28, 491.52, 368.64, 245.76	491.52	6

Table 13. Configuration Input Parameters

ITEM	PARAMETER	OPTIONS	COMMENTS		EXAMPLE
1	DAC Rate	5898, 4915, 4432, 3932, 3686, 2949, 2457	Value in Msps, must be used as given in the options column		4915
2	CLKPN Rate	983, 737, 491, 368, 307, 245	CLKP/CLKN clock rate in MHz	Device Clock = 1	491
		5898, 4915, 4423, 3932, 3686, 2949, 2457, 1474, 1228, 983, 737, 491, 368, 307, 245		Device Clock = 0	
3	INTP Ratio	4, 1	Interpolation Ratio		4
4	Lane Count	3, 4, 5, 6	Number of JESD204B lanes to be used		5
5	Subclass	0	JESD204B Subclass selection		0
6	Device Clock	0	JESD204B Frame sample clock derived from...	DAC clock	1
		1		CLKP/CLKN	

Table 13. Configuration Input Parameters (continued)

ITEM	PARAMETER	OPTIONS	COMMENTS		EXAMPLE
7	SYSREF Mode	0	SYSREF mode, set to 0		0
8	NCO Frequency	0, 1, ..., 2948, 2949	f_{NCO} in MHz, value between DC and the DAC Rate divided by 2		1000
9	RCLK Div	1, 2, 4	Sample-Rate-to-RCLK ratio		1
10	ScrambleDis	0	JESD204B lane scrambler	enabled	0
		1		disabled	

Example input file example_config.txt, contains the below parameter settings:

```
DAC Rate      = 4915
CLKPN Rate    = 491
INTP Ratio    = 4
Lane Count    = 5
Subclass      = 0
Device Clock  = 1
SYSREF Mode   = 0
NCO Freq      = 1000
RCLK Div      = 1
ScrambleDis   = 0
```

To execute the PERL script command line type the following:

```
perl gen_MAX585x_config.pl example_config.txt
```

Checking setup ...

```
Creating example_config.cfg file for following setup:
DAC update Rate.....4915 MHz
CLKPN Input Rate .....491 MHz
DSP INTP Ratio ..... 4
RxLink Lane Count ..... 5
RxLink Subclass ..... 0
RxLink Clock source ..... Device Clock
RxLink SYSREF mode .....One-shot
NCO Freq.....1000 MHz
RCLK Out..... Frame Rate/1
Scramble Disable.....0 (1:off, 0:on)
(SERDES = 10G, Full Rate; Frame Rate = 245.75M)
```

The resulting output command file can be used to configure the device through the SPI. Each line of the .cfg file contains the register address and the data value to be programmed. Within the output .cfg file, wait statements will be inserted at the required points in the programming sequence to indicate a need for a pause before the next write command.

The following is list of the first 7 lines of the example_config.cfg output file:

```
// For Trimmed version of part
// Script version used: v1.0
// SS:MIN:HR:DAY:MM:YY
// 21:12:11:26:10:17
0x0000,0xBD; //GLBL.CfgIFA.AddIncr=1'b1,
Wire4=1'b1, SftRst=1'b1 (self-clearing)
0x0010,0x05; //GLBL.CfgDACrate=4'b0101
0x0011,0x03; //GLBL.CfgCLKrate=4'b0011
```

Register Map

ADDRESS	NAME	MSB							LSB
GLBL									
0x00	CfgIFA[7:0]	SftRst	LSBF	AddIncr	Wire4	Wire4_0	AddIncr0	LSBF0	SftRst0
0x01	CfgIFB[7:0]	StrmDis	rsvd6	–	rsvd4	rsvd3	–	–	rsvd0
0x02	CfgDev[7:0]	rsvd[4:0]					CDrst	PDM[1:0]	
0x03	ChipType[7:0]	–	–	–	–	Type[3:0]			
0x04	ChipID1[7:0]	CIDLSB[1:0]		PID[1:0]		FID[3:0]			
0x05	ChipID2[7:0]	CIDMSB[7:0]							
0x06	ChipRev[7:0]	–	–	–	–	Rev[3:0]			
0x0C	VendID1[7:0]	VIDLSB[7:0]							
0x0D	VendID2[7:0]	VIDMSB[7:0]							
0x10	CfgDACrate[7:0]	–	–	–	–	Drate[3:0]			
0x11	CfgCLKrate[7:0]	–	–	–	–	Crate[3:0]			
0x12	CfgREGS[7:0]	–	–	–	–	–	–	rsvd	IntCfg
DSP									
0x100	CfgChipOM[7:0]	–	RclkM[1:0]		INVQ	–	Mute	–	DFMT
0x101	CfgDSP[7:0]	R[3:0]				RstDSP	RstFIFO	NCOE	NCOLD
0x102	CfgNCOF0[7:0]	FCW[7:0]							
0x103	CfgNCOF1[7:0]	FCW[15:8]							
0x104	CfgNCOF2[7:0]	FCW[23:16]							
0x105	CfgNCOF3[7:0]	FCW[31:24]							
0x106	CfgNCON0[7:0]	NFW[7:0]							
0x107	CfgNCON1[7:0]	NFW[15:8]							
0x108	CfgNCON2[7:0]	–	–	–	–	–	–	NFW[17:16]	
0x109	CfgNCOD0[7:0]	DFW[7:0]							
0x10A	CfgNCOD1[7:0]	DFW[15:8]							
0x10B	CfgNCOD2[7:0]	–	–	–	–	–	DFW[18:16]		
0x10C	CfgNCOU[7:0]	–	–	–	–	–	–	RLM[1:0]	
0x10D	CfgNCOUT0[7:0]	TIM[7:0]							
0x10E	CfgNCOUT1[7:0]	TIM[7:0]							
0x10F	CfgNCOUT2[7:0]	TIM[7:0]							
0x110	CfgPM[7:0]	–	–	–	–	–	Start	Mode	Reset
0x111	CfgPMT[7:0]	PMT[7:0]							
0x112	CfgPMIC0[7:0]	PMIC[7:0]							
0x113	CfgPMIC1[7:0]	PMIC[7:0]							
0x114	CfgPMIC2[7:0]	PMIC[7:0]							
0x115	CfgPMIC3[7:0]	PMIC[7:0]							
0x116	CfgPMIC4[7:0]	PMIC[7:0]							
0x117	CfgPMIC5[7:0]	PMIC[7:0]							
0x118	StatPM0[7:0]	PMST[7:0]							

ADDRESS	NAME	MSB							LSB
0x119	StatPM1[7:0]	PMDONE	–	–	–	PMST[3:0]			
0x15A	CfgSync[7:0]	–	ClkDiv_Sync	–	–	–	–	–	–
0x15B	CfgFIFO[7:0]	rsvd[4:0]					DupI	SwapIQ	RevBitOrd
0x15D	CfgRSV0[7:0]	RSV[7:0]							
0x15E	CfgRSV1[7:0]	RSV[7:0]							
0x15F	CfgRSV2[7:0]	RSV[7:0]							
0x160	CfgRSV3[7:0]	RSV[7:0]							
0x162	EMUTE[7:0]	EM[7:0]							
0x163	EINT[7:0]	INT_EN[7:0]							
0x164	STATUS[7:0]	JSDIM	JSDII	rsvd[2:0]			TRDY	–	PLLIck
0x165	RSVD7[7:0]	rsvd[7:0]							
0x166	DEVSN0[7:0]	SN[7:0]							
0x167	DEVSN1[7:0]	–	–	–	–	–	–	–	–
0x168	DEVSN2[7:0]	–	–	–	–	–	–	–	–
0x180	CfgPLL0[7:0]	–	–	–	–	–	–	–	MASTER
0x181	CfgPLL1[7:0]	–	PLL_BYP	DVAL0[1:0]		PVAL	RVAL0	–	–
0x182	CfgPLL2[7:0]	–	–	–	DVAL1[1:0]		RVAL1	–	VCO_SEL
0x183	StatPLL0[7:0]	rsvd[3:0]				PLL_LOCK	–	–	–
0x185	CfgClkDiv[7:0]	RDIV[3:0]				RSV[1:0]		PCLK[1:0]	
RLinkRegs									
0x400	CfgRLinkSet[31:24]	–	–	–	–	–	–	–	–
	CfgRLinkSet[23:16]	–	–	–	–	–	–	SyncInit	SyncPol
	CfgRLinkSet[15:8]	–	–	–	–	–	–	IgnDisp	ScrmD
	CfgRLinkSet[7:0]	–	–	DDiv[1:0]		Subclass[1:0]		RstSRL	RstILA
0x404	CfgRLinkParam1[31:24]	–	–	–	CfgS[4:0]				
	CfgRLinkParam1[23:16]	CfgF[7:0]							
	CfgRLinkParam1[15:8]	–	–	–	CfgL[4:0]				
	CfgRLinkParam1[7:0]	CfgM[7:0]							
0x408	CfgRLinkParam2[31:24]	DID[7:0]							
	CfgRLinkParam2[23:16]	HD	–	–	–	BID[3:0]			
	CfgRLinkParam2[15:8]	CfgNP[2:0]			CfgN[4:0]				
	CfgRLinkParam2[7:0]	–	–	–	CfgK[4:0]				
0x410	CfgRLinkCtrl[31:24]	–	–	–	–	–	–	–	–
	CfgRLinkCtrl[23:16]	–	SCtrl[1:0]		DFSync	–	–	–	–
	CfgRLinkCtrl[15:8]	–	–	–	–	–	–	–	SErrC
	CfgRLinkCtrl[7:0]	–	–	–	–	BitSwap	–	AsyncAvl	rclk
0x414	CfgRLinkMFrame[31:24]	–	–	–	–	–	–	SNum[8:7]	
	CfgRLinkMFrame[23:16]	SNum[6:0]							MFSel[8]
	CfgRLinkMFrame[15:8]	MFSel[7:0]							
	CfgRLinkMFrame[7:0]	–	–	ILADly[5:0]					

ADDRESS	NAME	MSB							LSB
0x418	CfgRSYNCN[31:24]	–	–	–	–	–	–	–	–
	CfgRSYNCN[23:16]	–	–	–	–	–	–	–	–
	CfgRSYNCN[15:8]	–	RepErr14	RepErr13	RepErr12	RepErr11	RepErr10	RepErr9	RepErr8
	CfgRSYNCN[7:0]	–	RepErr6	RepErr5	–	–	RepErr2	RepErr1	RepErr0
0x41C	CfgRFIFO[31:24]	–	–	–	–	–	–	–	–
	CfgRFIFO[23:16]	–	–	–	–	–	–	–	–
	CfgRFIFO[15:8]	–	–	–	MaxFD[4:0]				
	CfgRFIFO[7:0]	–	–	–	MinFD[4:0]				
0x420	CfgRTestCtrl[31:24]	–	–	–	–	–	–	–	LnCntType-Sel[3]
	CfgRTestCtrl[23:16]	LnCntTypeSel[2:0]			RxCntLaneSel[4:0]				
	CfgRTestCtrl[15:8]	–	–	SamLoad	RxLoad	CDcorEn	Rsvd0	–	–
	CfgRTestCtrl[7:0]	–	–	–	PRBStype[1:0]		–	RxPRBSen	SamPRB-S15En
0x424	CfgRLinkSTP1[31:24]	–	–	–	–	–	–	–	–
	CfgRLinkSTP1[23:16]	–	–	–	–	–	–	–	–
	CfgRLinkSTP1[15:8]	Sample1[15:8]							
	CfgRLinkSTP1[7:0]	Sample1[7:0]							
0x428	CfgRLinkSTP2[31:24]	–	–	–	–	–	–	–	–
	CfgRLinkSTP2[23:16]	–	–	–	–	–	–	–	–
	CfgRLinkSTP2[15:8]	Sample2[15:8]							
	CfgRLinkSTP2[7:0]	Sample2[7:0]							
0x430	CfgRLinkIntEn[31:24]	–	–	–	–	–	–	–	–
	CfgRLinkIntEn[23:16]	–	–	–	–	–	–	–	–
	CfgRLinkIntEn[15:8]	–	–	–	–	–	–	–	–
	CfgRLinkIntEn[7:0]	–	–	–	–	ILAnsync	–	–	ILAfail
0x434	CfgRLinkMuteEn[31:24]	–	–	–	–	–	–	–	–
	CfgRLinkMuteEn[23:16]	–	–	–	–	–	–	–	–
	CfgRLinkMuteEn[15:8]	–	–	–	–	–	–	–	–
	CfgRLinkMuteEn[7:0]	–	–	–	–	ILAnsync	–	–	ILAfail
0x438	StatRLinkILA[31:24]	–	–	–	–	–	–	–	–
	StatRLinkILA[23:16]	–	–	–	–	–	–	–	–
	StatRLinkILA[15:8]	–	–	–	–	–	–	–	–
	StatRLinkILA[7:0]	–	–	–	–	ILAnsync	–	–	ILAfailure
0x43C	StatRLinkSTP[31:24]	–	–	–	–	–	–	–	–
	StatRLinkSTP[23:16]	–	–	–	–	–	–	–	–
	StatRLinkSTP[15:8]	–	–	–	–	–	–	–	–
	StatRLinkSTP[7:0]	–	–	–	–	–	–	STPerr1	STPerr0

ADDRESS	NAME	MSB							LSB
0x440	StatRLinkPRBS[31:24]	–	–	–	–	–	–	–	–
	StatRLinkPRBS[23:16]	–	–	–	–	–	–	–	–
	StatRLinkPRBS[15:8]	–	–	–	–	–	–	–	–
	StatRLinkPRBS[7:0]	–	–	–	–	–	–	PRBSerr1	PRBSerr0
0x460	CntRLaneInvld[31:24]	–	–	–	–	–	–	–	–
	CntRLaneInvld[23:16]	–	–	–	–	–	–	–	–
	CntRLaneInvld[15:8]	InvCnt[15:8]							
	CntRLaneInvld[7:0]	InvCnt[7:0]							
0x464	CntRLaneDbg[31:24]	–	–	–	–	–	–	–	–
	CntRLaneDbg[23:16]	–	–	–	–	–	–	–	–
	CntRLaneDbg[15:8]	DbgCnt[15:8]							
	CntRLaneDbg[7:0]	DbgCnt[7:0]							
RLaneRegs 0									
0x480	CfgRLaneSet[31:24]	LnSrc[4:0]					–	LkSel	LnEn
	CfgRLaneSet[23:16]	–	–	–	–	–	–	–	–
	CfgRLaneSet[15:8]	–	–	–	–	–	–	–	–
	CfgRLaneSet[7:0]	–	–	LID[4:0]					LnRst
0x484	CfgRLaneIntEn[31:24]	–	DContErr	–	PRBSerr	KContErr	FChkErr	LCfgErr	ILAerr
	CfgRLaneIntEn[23:16]	–	–	–	–	–	–	FIFOempty	FIFOfull
	CfgRLaneIntEn[15:8]	–	–	–	–	–	–	–	–
	CfgRLaneIntEn[7:0]	FrNSync	LnReAlign	FrReAlign	–	–	DISP	NIT	CGS
0x488	CfgRLaneMuteEn[31:24]	–	DContErr	–	PRBSerr	KContErr	FChkErr	LCfgErr	ILAerr
	CfgRLaneMuteEn[23:16]	–	–	–	–	–	–	FIFOempty	FIFOfull
	CfgRLaneMuteEn[15:8]	–	–	–	–	–	–	–	–
	CfgRLaneMuteEn[7:0]	FrNSync	LnReAlign	FrReAlign	–	–	DISP	NIT	CGS
0x48C	StatRLane[31:24]	–	DContErr	–	PRBSerr	KContErr	FChkErr	LCfgErr	ILAerr
	StatRLane[23:16]	–	–	–	–	–	–	FIFOempty	FIFOfull
	StatRLane[15:8]	–	–	FIFODepth[5:0]					
	StatRLane[7:0]	FrNSync	LnReAlign	FrReAlign	–	–	DISP	NIT	CGS
RLaneRegs 1									
0x490	CfgRLaneSet[31:24]	LnSrc[4:0]					–	LkSel	LnEn
	CfgRLaneSet[23:16]	–	–	–	–	–	–	–	–
	CfgRLaneSet[15:8]	–	–	–	–	–	–	–	–
	CfgRLaneSet[7:0]	–	–	LID[4:0]					LnRst
0x494	CfgRLaneIntEn[31:24]	–	DContErr	–	PRBSerr	KContErr	FChkErr	LCfgErr	ILAerr
	CfgRLaneIntEn[23:16]	–	–	–	–	–	–	FIFOempty	FIFOfull
	CfgRLaneIntEn[15:8]	–	–	–	–	–	–	–	–
	CfgRLaneIntEn[7:0]	FrNSync	LnReAlign	FrReAlign	–	–	DISP	NIT	CGS

ADDRESS	NAME	MSB							LSB
0x498	CfgRLaneMuteEn[31:24]	–	DContErr	–	PRBSerr	KContErr	FChkErr	LCfgErr	ILAerr
	CfgRLaneMuteEn[23:16]	–	–	–	–	–	–	FIFOempty	FIFOfull
	CfgRLaneMuteEn[15:8]	–	–	–	–	–	–	–	–
	CfgRLaneMuteEn[7:0]	FrNSync	LnReAlign	FrReAlign	–	–	DISP	NIT	CGS
0x49C	StatRLane[31:24]	–	DContErr	–	PRBSerr	KContErr	FChkErr	LCfgErr	ILAerr
	StatRLane[23:16]	–	–	–	–	–	–	FIFOempty	FIFOfull
	StatRLane[15:8]	–	–	FIFODepth[5:0]					
	StatRLane[7:0]	FrNSync	LnReAlign	FrReAlign	–	–	DISP	NIT	CGS
RLaneRegs 2									
0x4A0	CfgRLaneSet[31:24]	LnSrc[4:0]					–	LkSel	LnEn
	CfgRLaneSet[23:16]	–	–	–	–	–	–	–	–
	CfgRLaneSet[15:8]	–	–	–	–	–	–	–	–
	CfgRLaneSet[7:0]	–	–	LID[4:0]					LnRst
0x4A4	CfgRLaneIntEn[31:24]	–	DContErr	–	PRBSerr	KContErr	FChkErr	LCfgErr	ILAerr
	CfgRLaneIntEn[23:16]	–	–	–	–	–	–	FIFOempty	FIFOfull
	CfgRLaneIntEn[15:8]	–	–	–	–	–	–	–	–
	CfgRLaneIntEn[7:0]	FrNSync	LnReAlign	FrReAlign	–	–	DISP	NIT	CGS
0x4A8	CfgRLaneMuteEn[31:24]	–	DContErr	–	PRBSerr	KContErr	FChkErr	LCfgErr	ILAerr
	CfgRLaneMuteEn[23:16]	–	–	–	–	–	–	FIFOempty	FIFOfull
	CfgRLaneMuteEn[15:8]	–	–	–	–	–	–	–	–
	CfgRLaneMuteEn[7:0]	FrNSync	LnReAlign	FrReAlign	–	–	DISP	NIT	CGS
0x4AC	StatRLane[31:24]	–	DContErr	–	PRBSerr	KContErr	FChkErr	LCfgErr	ILAerr
	StatRLane[23:16]	–	–	–	–	–	–	FIFOempty	FIFOfull
	StatRLane[15:8]	–	–	FIFODepth[5:0]					
	StatRLane[7:0]	FrNSync	LnReAlign	FrReAlign	–	–	DISP	NIT	CGS
RLaneRegs 3									
0x4B0	CfgRLaneSet[31:24]	LnSrc[4:0]					–	LkSel	LnEn
	CfgRLaneSet[23:16]	–	–	–	–	–	–	–	–
	CfgRLaneSet[15:8]	–	–	–	–	–	–	–	–
	CfgRLaneSet[7:0]	–	–	LID[4:0]					LnRst
0x4B4	CfgRLaneIntEn[31:24]	–	DContErr	–	PRBSerr	KContErr	FChkErr	LCfgErr	ILAerr
	CfgRLaneIntEn[23:16]	–	–	–	–	–	–	FIFOempty	FIFOfull
	CfgRLaneIntEn[15:8]	–	–	–	–	–	–	–	–
	CfgRLaneIntEn[7:0]	FrNSync	LnReAlign	FrReAlign	–	–	DISP	NIT	CGS
0x4B8	CfgRLaneMuteEn[31:24]	–	DContErr	–	PRBSerr	KContErr	FChkErr	LCfgErr	ILAerr
	CfgRLaneMuteEn[23:16]	–	–	–	–	–	–	FIFOempty	FIFOfull
	CfgRLaneMuteEn[15:8]	–	–	–	–	–	–	–	–
	CfgRLaneMuteEn[7:0]	FrNSync	LnReAlign	FrReAlign	–	–	DISP	NIT	CGS

ADDRESS	NAME	MSB							LSB
0x4BC	StatRLane[31:24]	–	DContErr	–	PRBSerr	KContErr	FChkErr	LCfgErr	ILAerr
	StatRLane[23:16]	–	–	–	–	–	–	FIFOempty	FIFOfull
	StatRLane[15:8]	–	–	FIFODepth[5:0]					
	StatRLane[7:0]	FrNSync	LnReAlign	FrReAlign	–	–	DISP	NIT	CGS
RLaneRegs 4									
0x4C0	CfgRLaneSet[31:24]	LnSrc[4:0]					–	LkSel	LnEn
	CfgRLaneSet[23:16]	–	–	–	–	–	–	–	–
	CfgRLaneSet[15:8]	–	–	–	–	–	–	–	–
	CfgRLaneSet[7:0]	–	–	LID[4:0]					LnRst
0x4C4	CfgRLaneIntEn[31:24]	–	DContErr	–	PRBSerr	KContErr	FChkErr	LCfgErr	ILAerr
	CfgRLaneIntEn[23:16]	–	–	–	–	–	–	FIFOempty	FIFOfull
	CfgRLaneIntEn[15:8]	–	–	–	–	–	–	–	–
	CfgRLaneIntEn[7:0]	FrNSync	LnReAlign	FrReAlign	–	–	DISP	NIT	CGS
0x4C8	CfgRLaneMuteEn[31:24]	–	DContErr	–	PRBSerr	KContErr	FChkErr	LCfgErr	ILAerr
	CfgRLaneMuteEn[23:16]	–	–	–	–	–	–	FIFOempty	FIFOfull
	CfgRLaneMuteEn[15:8]	–	–	–	–	–	–	–	–
	CfgRLaneMuteEn[7:0]	FrNSync	LnReAlign	FrReAlign	–	–	DISP	NIT	CGS
0x4CC	StatRLane[31:24]	–	DContErr	–	PRBSerr	KContErr	FChkErr	LCfgErr	ILAerr
	StatRLane[23:16]	–	–	–	–	–	–	FIFOempty	FIFOfull
	StatRLane[15:8]	–	–	FIFODepth[5:0]					
	StatRLane[7:0]	FrNSync	LnReAlign	FrReAlign	–	–	DISP	NIT	CGS
RLaneRegs 5									
0x4D0	CfgRLaneSet[31:24]	LnSrc[4:0]					–	LkSel	LnEn
	CfgRLaneSet[23:16]	–	–	–	–	–	–	–	–
	CfgRLaneSet[15:8]	–	–	–	–	–	–	–	–
	CfgRLaneSet[7:0]	–	–	LID[4:0]					LnRst
0x4D4	CfgRLaneIntEn[31:24]	–	DContErr	–	PRBSerr	KContErr	FChkErr	LCfgErr	ILAerr
	CfgRLaneIntEn[23:16]	–	–	–	–	–	–	FIFOempty	FIFOfull
	CfgRLaneIntEn[15:8]	–	–	–	–	–	–	–	–
	CfgRLaneIntEn[7:0]	FrNSync	LnReAlign	FrReAlign	–	–	DISP	NIT	CGS
0x4D8	CfgRLaneMuteEn[31:24]	–	DContErr	–	PRBSerr	KContErr	FChkErr	LCfgErr	ILAerr
	CfgRLaneMuteEn[23:16]	–	–	–	–	–	–	FIFOempty	FIFOfull
	CfgRLaneMuteEn[15:8]	–	–	–	–	–	–	–	–
	CfgRLaneMuteEn[7:0]	FrNSync	LnReAlign	FrReAlign	–	–	DISP	NIT	CGS
0x4DC	StatRLane[31:24]	–	DContErr	–	PRBSerr	KContErr	FChkErr	LCfgErr	ILAerr
	StatRLane[23:16]	–	–	–	–	–	–	FIFOempty	FIFOfull
	StatRLane[15:8]	–	–	FIFODepth[5:0]					
	StatRLane[7:0]	FrNSync	LnReAlign	FrReAlign	–	–	DISP	NIT	CGS

ADDRESS	NAME	MSB							LSB
SerDesRegs									
0x600	CfgSerDes[31:24]	–	–	–	–	–	–	–	–
	CfgSerDes[23:16]	–	–	–	–	–	–	RxRateSel[1:0]	
	CfgSerDes[15:8]	–	–	–	–	–	–	–	–
	CfgSerDes[7:0]	PhyWMode[1:0]		BCast[1:0]		–	PhyKill	–	Rst
0x608	CfgTrainAct[31:24]	–	–	–	–	–	–	–	–
	CfgTrainAct[23:16]	–	–	–	–	–	–	–	–
	CfgTrainAct[15:8]	–	–	–	–	–	–	–	–
	CfgTrainAct[7:0]	–	–	Ln__5	Ln__4	Ln__3	Ln__2	Ln__1	Ln__0
0x60C	CfgTrainDeAct[31:24]	–	–	–	–	–	–	–	–
	CfgTrainDeAct[23:16]	–	–	–	–	–	–	–	–
	CfgTrainDeAct[15:8]	–	–	–	–	–	–	–	–
	CfgTrainDeAct[7:0]	–	–	Ln__5	Ln__4	Ln__3	Ln__2	Ln__1	Ln__0
0x610	CfgIdleGate[31:24]	–	–	–	–	–	–	–	–
	CfgIdleGate[23:16]	–	–	–	–	–	–	–	–
	CfgIdleGate[15:8]	–	–	–	–	–	–	–	–
	CfgIdleGate[7:0]	–	–	Ln__5	Ln__4	Ln__3	Ln__2	Ln__1	Ln__0
0x614	CfgDoneGate[31:24]	–	–	–	–	–	–	–	–
	CfgDoneGate[23:16]	–	–	–	–	–	–	–	–
	CfgDoneGate[15:8]	–	–	–	–	–	–	–	–
	CfgDoneGate[7:0]	–	–	Ln__5	Ln__4	Ln__3	Ln__2	Ln__1	Ln__0
0x618	CfgReserved[31:24]	–	–	–	–	–	–	–	–
	CfgReserved[23:16]	–	–	–	–	–	–	–	–
	CfgReserved[15:8]	Rsvd[15:8]							
	CfgReserved[7:0]	Rsvd[7:0]							
0x61C	CfgIntEnRLMS[31:24]	–	–	–	–	–	–	–	–
	CfgIntEnRLMS[23:16]	–	–	–	–	–	–	–	–
	CfgIntEnRLMS[15:8]	–	–	–	–	–	–	–	–
	CfgIntEnRLMS[7:0]	–	–	Ln__5	Ln__4	Ln__3	Ln__2	Ln__1	Ln__0
0x620	CfgIntEnTrainDn[31:24]	–	–	–	–	–	–	–	–
	CfgIntEnTrainDn[23:16]	–	–	–	–	–	–	–	–
	CfgIntEnTrainDn[15:8]	–	–	–	–	–	–	–	–
	CfgIntEnTrainDn[7:0]	–	–	Ln__5	Ln__4	Ln__3	Ln__2	Ln__1	Ln__0
0x624	CfgIntEnSigDet[31:24]	–	–	–	–	–	–	–	–
	CfgIntEnSigDet[23:16]	–	–	–	–	–	–	–	–
	CfgIntEnSigDet[15:8]	–	–	–	–	–	–	–	–
	CfgIntEnSigDet[7:0]	–	–	Ln__5	Ln__4	Ln__3	Ln__2	Ln__1	Ln__0

ADDRESS	NAME	MSB							LSB
0x628	CfgMuteEnRLMS[31:24]	–	–	–	–	–	–	–	–
	CfgMuteEnRLMS[23:16]	–	–	–	–	–	–	–	–
	CfgMuteEnRLMS[15:8]	–	–	–	–	–	–	–	–
	CfgMuteEnRLMS[7:0]	–	–	Ln__5	Ln__4	Ln__3	Ln__2	Ln__1	Ln__0
0x62C	CfgMuteEnTrainDn[31:24]	–	–	–	–	–	–	–	–
	CfgMuteEnTrainDn[23:16]	–	–	–	–	–	–	–	–
	CfgMuteEnTrainDn[15:8]	–	–	–	–	–	–	–	–
	CfgMuteEnTrainDn[7:0]	–	–	Ln__5	Ln__4	Ln__3	Ln__2	Ln__1	Ln__0
0x630	CfgMuteEnSigDet[31:24]	–	–	–	–	–	–	–	–
	CfgMuteEnSigDet[23:16]	–	–	–	–	–	–	–	–
	CfgMuteEnSigDet[15:8]	–	–	–	–	–	–	–	–
	CfgMuteEnSigDet[7:0]	–	–	Ln__5	Ln__4	Ln__3	Ln__2	Ln__1	Ln__0
0x634	StatRLMS[31:24]	–	–	–	–	–	–	–	–
	StatRLMS[23:16]	–	–	–	–	–	–	–	–
	StatRLMS[15:8]	–	–	–	–	–	–	–	–
	StatRLMS[7:0]	–	–	Ln__5	Ln__4	Ln__3	Ln__2	Ln__1	Ln__0
0x638	StatTrainDn[31:24]	–	–	–	–	–	–	–	–
	StatTrainDn[23:16]	–	–	–	–	–	–	–	–
	StatTrainDn[15:8]	–	–	–	–	–	–	–	–
	StatTrainDn[7:0]	–	–	Ln__5	Ln__4	Ln__3	Ln__2	Ln__1	Ln__0
0x63C	StatSigDet[31:24]	–	–	–	–	–	–	–	–
	StatSigDet[23:16]	–	–	–	–	–	–	–	–
	StatSigDet[15:8]	–	–	–	–	–	–	–	–
	StatSigDet[7:0]	–	–	Ln__5	Ln__4	Ln__3	Ln__2	Ln__1	Ln__0
CMURegs									
0x644	CfgCMU1[31:24]	Rsvd1	–	–	–	–	cd_tune1p0[2:0]		
	CfgCMU1[23:16]	Cref_divsel1p0[1:0]		–	–	Rsvd0[13:10]			
	CfgCMU1[15:8]	Rsvd0[9:2]							
	CfgCMU1[7:0]	Rsvd0[1:0]		FBDIV[1:0]		VCOSEL[1:0]		–	–
PHY 0									
0x80C	EQU_CTRL3[31:24]	Reserved[1:0]		D1_coeff[5:0]					
	EQU_CTRL3[23:16]	Reserved	D2_coeff[6:0]						
	EQU_CTRL3[15:8]	Reserved	D3_coeff[6:0]						
	EQU_CTRL3[7:0]	Reserved	D4_coeff[6:0]						
0x810	EQU_CTRL4[31:24]	Reserved	Reserved[6:0]						
	EQU_CTRL4[23:16]	Reserved[9:2]							
	EQU_CTRL4[15:8]	Reserved[1:0]		Reserved[5:0]					
	EQU_CTRL4[7:0]	AGC_coeff[7:0]							

ADDRESS	NAME	MSB							LSB
0x81C	EQU_CTRL7[31:24]	AGC_init_D1[7:0]							
	EQU_CTRL7[23:16]	Reserved[7:0]							
	EQU_CTRL7[15:8]	Reserved[1:0]		Reserved[5:0]					
	EQU_CTRL7[7:0]	Reserved[7:0]							
0x828	EQU_CTRLA[31:24]	Reserved[1:0]		D1_init[5:0]					
	EQU_CTRLA[23:16]	Reserved	D2_init[6:0]						
	EQU_CTRLA[15:8]	Reserved	D3_init[6:0]						
	EQU_CTRLA[7:0]	Reserved	D4_init[6:0]						
0x82C	EQU_CTRLB[31:24]	Reserved[1:0]		Reserved[1:0]		capsel[1:0]		Mode6Gphb	Reserved
	EQU_CTRLB[23:16]	Reserved[1:0]		Reserved[5:0]					
	EQU_CTRLB[15:8]	Reserved[7:0]							
	EQU_CTRLB[7:0]	Reserved[7:0]							
0x83C	EYE_MON2[31:24]	D1ErrChPhPri[7:0]							
	EYE_MON2[23:16]	D1ErrChPhSec[7:0]							
	EYE_MON2[15:8]	Reserved[7:0]							
	EYE_MON2[7:0]	Reserved	Reserved[6:0]						
0x864	CLK_CTRL1[31:24]	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
	CLK_CTRL1[23:16]	Reserved	Reserved	Reserved	Reserved	Reserved[3:0]			
	CLK_CTRL1[15:8]	Reserved[3:0]				Reserved	cd_tune[2:0]		
	CLK_CTRL1[7:0]	Reserved[3:0]				Reserved	Reserved	Reserved[1:0]	
0x880	EQU_CTRLD[31:24]	Reserved[1:0]		DFE2_initD3[5:0]					
	EQU_CTRLD[23:16]	Reserved	DFE2_initD2[6:0]						
	EQU_CTRLD[15:8]	Reserved	DFE1_initD3[6:0]						
	EQU_CTRLD[7:0]	Reserved	DFE1_initD2[6:0]						
0x884	EQU_CTRLE[31:24]	Reserved	DFE4Init_D3[6:0]						
	EQU_CTRLE[23:16]	Reserved	DFE4Init_D2[6:0]						
	EQU_CTRLE[15:8]	Reserved	DFE3Init_D3[6:0]						
	EQU_CTRLE[7:0]	Reserved	DFE3Init_D2[6:0]						
0x88C	EQU_CTRLG[31:24]	Reserved[7:0]							
	EQU_CTRLG[23:16]	Reserved[7:0]							
	EQU_CTRLG[15:8]	AGCInit_D3[7:0]							
	EQU_CTRLG[7:0]	AGCInit_D2[7:0]							
PHY 1									
0x90C	EQU_CTRL3[31:24]	Reserved[1:0]		D1_coeff[5:0]					
	EQU_CTRL3[23:16]	Reserved	D2_coeff[6:0]						
	EQU_CTRL3[15:8]	Reserved	D3_coeff[6:0]						
	EQU_CTRL3[7:0]	Reserved	D4_coeff[6:0]						
0x910	EQU_CTRL4[31:24]	Reserved	Reserved[6:0]						
	EQU_CTRL4[23:16]	Reserved[9:2]							
	EQU_CTRL4[15:8]	Reserved[1:0]		Reserved[5:0]					
	EQU_CTRL4[7:0]	AGC_coeff[7:0]							

ADDRESS	NAME	MSB							LSB
0x91C	EQU_CTRL7[31:24]	AGC_init_D1[7:0]							
	EQU_CTRL7[23:16]	Reserved[7:0]							
	EQU_CTRL7[15:8]	Reserved[1:0]		Reserved[5:0]					
	EQU_CTRL7[7:0]	Reserved[7:0]							
0x928	EQU_CTRLA[31:24]	Reserved[1:0]		D1_init[5:0]					
	EQU_CTRLA[23:16]	Reserved	D2_init[6:0]						
	EQU_CTRLA[15:8]	Reserved	D3_init[6:0]						
	EQU_CTRLA[7:0]	Reserved	D4_init[6:0]						
0x92C	EQU_CTRLB[31:24]	Reserved[1:0]		Reserved[1:0]		capsel[1:0]		Mode6Gphb	Reserved
	EQU_CTRLB[23:16]	Reserved[1:0]		Reserved[5:0]					
	EQU_CTRLB[15:8]	Reserved[7:0]							
	EQU_CTRLB[7:0]	Reserved[7:0]							
0x93C	EYE_MON2[31:24]	D1ErrChPhPri[7:0]							
	EYE_MON2[23:16]	D1ErrChPhSec[7:0]							
	EYE_MON2[15:8]	Reserved[7:0]							
	EYE_MON2[7:0]	Reserved	Reserved[6:0]						
0x964	CLK_CTRL1[31:24]	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
	CLK_CTRL1[23:16]	Reserved	Reserved	Reserved	Reserved	Reserved[3:0]			
	CLK_CTRL1[15:8]	Reserved[3:0]				Reserved	cd_tune[2:0]		
	CLK_CTRL1[7:0]	Reserved[3:0]				Reserved	Reserved	Reserved[1:0]	
0x980	EQU_CTRLD[31:24]	Reserved[1:0]		DFE2_initD3[5:0]					
	EQU_CTRLD[23:16]	Reserved	DFE2_initD2[6:0]						
	EQU_CTRLD[15:8]	Reserved	DFE1_initD3[6:0]						
	EQU_CTRLD[7:0]	Reserved	DFE1_initD2[6:0]						
0x984	EQU_CTRLE[31:24]	Reserved	DFE4Init_D3[6:0]						
	EQU_CTRLE[23:16]	Reserved	DFE4Init_D2[6:0]						
	EQU_CTRLE[15:8]	Reserved	DFE3Init_D3[6:0]						
	EQU_CTRLE[7:0]	Reserved	DFE3Init_D2[6:0]						
0x98C	EQU_CTRLG[31:24]	Reserved[7:0]							
	EQU_CTRLG[23:16]	Reserved[7:0]							
	EQU_CTRLG[15:8]	AGCInit_D3[7:0]							
	EQU_CTRLG[7:0]	AGCInit_D2[7:0]							
PHY 2									
0xA0C	EQU_CTRL3[31:24]	Reserved[1:0]		D1_coeff[5:0]					
	EQU_CTRL3[23:16]	Reserved	D2_coeff[6:0]						
	EQU_CTRL3[15:8]	Reserved	D3_coeff[6:0]						
	EQU_CTRL3[7:0]	Reserved	D4_coeff[6:0]						
0xA10	EQU_CTRL4[31:24]	Reserved	Reserved[6:0]						
	EQU_CTRL4[23:16]	Reserved[9:2]							
	EQU_CTRL4[15:8]	Reserved[1:0]		Reserved[5:0]					
	EQU_CTRL4[7:0]	AGC_coeff[7:0]							

ADDRESS	NAME	MSB							LSB
0xA1C	EQU_CTRL7[31:24]	AGC_init_D1[7:0]							
	EQU_CTRL7[23:16]	Reserved[7:0]							
	EQU_CTRL7[15:8]	Reserved[1:0]		Reserved[5:0]					
	EQU_CTRL7[7:0]	Reserved[7:0]							
0xA28	EQU_CTRLA[31:24]	Reserved[1:0]		D1_init[5:0]					
	EQU_CTRLA[23:16]	Reserved	D2_init[6:0]						
	EQU_CTRLA[15:8]	Reserved	D3_init[6:0]						
	EQU_CTRLA[7:0]	Reserved	D4_init[6:0]						
0xA2C	EQU_CTRLB[31:24]	Reserved[1:0]		Reserved[1:0]		capsel[1:0]		Mode6Gphb	Reserved
	EQU_CTRLB[23:16]	Reserved[1:0]		Reserved[5:0]					
	EQU_CTRLB[15:8]	Reserved[7:0]							
	EQU_CTRLB[7:0]	Reserved[7:0]							
0xA3C	EYE_MON2[31:24]	D1ErrChPhPri[7:0]							
	EYE_MON2[23:16]	D1ErrChPhSec[7:0]							
	EYE_MON2[15:8]	Reserved[7:0]							
	EYE_MON2[7:0]	Reserved	Reserved[6:0]						
0xA64	CLK_CTRL1[31:24]	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
	CLK_CTRL1[23:16]	Reserved	Reserved	Reserved	Reserved	Reserved[3:0]			
	CLK_CTRL1[15:8]	Reserved[3:0]				Reserved	cd_tune[2:0]		
	CLK_CTRL1[7:0]	Reserved[3:0]				Reserved	Reserved	Reserved[1:0]	
0xA80	EQU_CTRLD[31:24]	Reserved[1:0]		DFE2_initD3[5:0]					
	EQU_CTRLD[23:16]	Reserved	DFE2_initD2[6:0]						
	EQU_CTRLD[15:8]	Reserved	DFE1_initD3[6:0]						
	EQU_CTRLD[7:0]	Reserved	DFE1_initD2[6:0]						
0xA84	EQU_CTRLE[31:24]	Reserved	DFE4Init_D3[6:0]						
	EQU_CTRLE[23:16]	Reserved	DFE4Init_D2[6:0]						
	EQU_CTRLE[15:8]	Reserved	DFE3Init_D3[6:0]						
	EQU_CTRLE[7:0]	Reserved	DFE3Init_D2[6:0]						
0xA8C	EQU_CTRLG[31:24]	Reserved[7:0]							
	EQU_CTRLG[23:16]	Reserved[7:0]							
	EQU_CTRLG[15:8]	AGCInit_D3[7:0]							
	EQU_CTRLG[7:0]	AGCInit_D2[7:0]							
PHY 3									
0xB0C	EQU_CTRL3[31:24]	Reserved[1:0]		D1_coeff[5:0]					
	EQU_CTRL3[23:16]	Reserved	D2_coeff[6:0]						
	EQU_CTRL3[15:8]	Reserved	D3_coeff[6:0]						
	EQU_CTRL3[7:0]	Reserved	D4_coeff[6:0]						
0xB10	EQU_CTRL4[31:24]	Reserved	Reserved[6:0]						
	EQU_CTRL4[23:16]	Reserved[9:2]							
	EQU_CTRL4[15:8]	Reserved[1:0]		Reserved[5:0]					
	EQU_CTRL4[7:0]	AGC_coeff[7:0]							

ADDRESS	NAME	MSB							LSB
0xB1C	EQU_CTRL7[31:24]	AGC_init_D1[7:0]							
	EQU_CTRL7[23:16]	Reserved[7:0]							
	EQU_CTRL7[15:8]	Reserved[1:0]		Reserved[5:0]					
	EQU_CTRL7[7:0]	Reserved[7:0]							
0xB28	EQU_CTRLA[31:24]	Reserved[1:0]		D1_init[5:0]					
	EQU_CTRLA[23:16]	Reserved	D2_init[6:0]						
	EQU_CTRLA[15:8]	Reserved	D3_init[6:0]						
	EQU_CTRLA[7:0]	Reserved	D4_init[6:0]						
0xB2C	EQU_CTRLB[31:24]	Reserved[1:0]		Reserved[1:0]		capsel[1:0]		Mode6Gphb	Reserved
	EQU_CTRLB[23:16]	Reserved[1:0]		Reserved[5:0]					
	EQU_CTRLB[15:8]	Reserved[7:0]							
	EQU_CTRLB[7:0]	Reserved[7:0]							
0xB3C	EYE_MON2[31:24]	D1ErrChPhPri[7:0]							
	EYE_MON2[23:16]	D1ErrChPhSec[7:0]							
	EYE_MON2[15:8]	Reserved[7:0]							
	EYE_MON2[7:0]	Reserved	Reserved[6:0]						
0xB64	CLK_CTRL1[31:24]	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
	CLK_CTRL1[23:16]	Reserved	Reserved	Reserved	Reserved	Reserved[3:0]			
	CLK_CTRL1[15:8]	Reserved[3:0]				Reserved	cd_tune[2:0]		
	CLK_CTRL1[7:0]	Reserved[3:0]				Reserved	Reserved	Reserved[1:0]	
0xB80	EQU_CTRLD[31:24]	Reserved[1:0]		DFE2_initD3[5:0]					
	EQU_CTRLD[23:16]	Reserved	DFE2_initD2[6:0]						
	EQU_CTRLD[15:8]	Reserved	DFE1_initD3[6:0]						
	EQU_CTRLD[7:0]	Reserved	DFE1_initD2[6:0]						
0xB84	EQU_CTRLE[31:24]	Reserved	DFE4Init_D3[6:0]						
	EQU_CTRLE[23:16]	Reserved	DFE4Init_D2[6:0]						
	EQU_CTRLE[15:8]	Reserved	DFE3Init_D3[6:0]						
	EQU_CTRLE[7:0]	Reserved	DFE3Init_D2[6:0]						
0xB8C	EQU_CTRLG[31:24]	Reserved[7:0]							
	EQU_CTRLG[23:16]	Reserved[7:0]							
	EQU_CTRLG[15:8]	AGCInit_D3[7:0]							
	EQU_CTRLG[7:0]	AGCInit_D2[7:0]							
PHY 4									
0xC0C	EQU_CTRL3[31:24]	Reserved[1:0]		D1_coeff[5:0]					
	EQU_CTRL3[23:16]	Reserved	D2_coeff[6:0]						
	EQU_CTRL3[15:8]	Reserved	D3_coeff[6:0]						
	EQU_CTRL3[7:0]	Reserved	D4_coeff[6:0]						
0xC10	EQU_CTRL4[31:24]	Reserved	Reserved[6:0]						
	EQU_CTRL4[23:16]	Reserved[9:2]							
	EQU_CTRL4[15:8]	Reserved[1:0]		Reserved[5:0]					
	EQU_CTRL4[7:0]	AGC_coeff[7:0]							

ADDRESS	NAME	MSB							LSB
0xC1C	EQU_CTRL7[31:24]	AGC_init_D1[7:0]							
	EQU_CTRL7[23:16]	Reserved[7:0]							
	EQU_CTRL7[15:8]	Reserved[1:0]		Reserved[5:0]					
	EQU_CTRL7[7:0]	Reserved[7:0]							
0xC28	EQU_CTRLA[31:24]	Reserved[1:0]		D1_init[5:0]					
	EQU_CTRLA[23:16]	Reserved	D2_init[6:0]						
	EQU_CTRLA[15:8]	Reserved	D3_init[6:0]						
	EQU_CTRLA[7:0]	Reserved	D4_init[6:0]						
0xC2C	EQU_CTRLB[31:24]	Reserved[1:0]		Reserved[1:0]		capsel[1:0]		Mode6Gphb	Reserved
	EQU_CTRLB[23:16]	Reserved[1:0]		Reserved[5:0]					
	EQU_CTRLB[15:8]	Reserved[7:0]							
	EQU_CTRLB[7:0]	Reserved[7:0]							
0xC3C	EYE_MON2[31:24]	D1ErrChPhPri[7:0]							
	EYE_MON2[23:16]	D1ErrChPhSec[7:0]							
	EYE_MON2[15:8]	Reserved[7:0]							
	EYE_MON2[7:0]	Reserved	Reserved[6:0]						
0xC64	CLK_CTRL1[31:24]	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
	CLK_CTRL1[23:16]	Reserved	Reserved	Reserved	Reserved	Reserved[3:0]			
	CLK_CTRL1[15:8]	Reserved[3:0]				Reserved	cd_tune[2:0]		
	CLK_CTRL1[7:0]	Reserved[3:0]				Reserved	Reserved	Reserved[1:0]	
0xC80	EQU_CTRLD[31:24]	Reserved[1:0]		DFE2_initD3[5:0]					
	EQU_CTRLD[23:16]	Reserved	DFE2_initD2[6:0]						
	EQU_CTRLD[15:8]	Reserved	DFE1_initD3[6:0]						
	EQU_CTRLD[7:0]	Reserved	DFE1_initD2[6:0]						
0xC84	EQU_CTRLE[31:24]	Reserved	DFE4Init_D3[6:0]						
	EQU_CTRLE[23:16]	Reserved	DFE4Init_D2[6:0]						
	EQU_CTRLE[15:8]	Reserved	DFE3Init_D3[6:0]						
	EQU_CTRLE[7:0]	Reserved	DFE3Init_D2[6:0]						
0xC8C	EQU_CTRLG[31:24]	Reserved[7:0]							
	EQU_CTRLG[23:16]	Reserved[7:0]							
	EQU_CTRLG[15:8]	AGCInit_D3[7:0]							
	EQU_CTRLG[7:0]	AGCInit_D2[7:0]							
PHY 5									
0xD0C	EQU_CTRL3[31:24]	Reserved[1:0]		D1_coeff[5:0]					
	EQU_CTRL3[23:16]	Reserved	D2_coeff[6:0]						
	EQU_CTRL3[15:8]	Reserved	D3_coeff[6:0]						
	EQU_CTRL3[7:0]	Reserved	D4_coeff[6:0]						
0xD10	EQU_CTRL4[31:24]	Reserved	Reserved[6:0]						
	EQU_CTRL4[23:16]	Reserved[9:2]							
	EQU_CTRL4[15:8]	Reserved[1:0]		Reserved[5:0]					
	EQU_CTRL4[7:0]	AGC_coeff[7:0]							

ADDRESS	NAME	MSB							LSB
0xD1C	EQU_CTRL7[31:24]	AGC_init_D1[7:0]							
	EQU_CTRL7[23:16]	Reserved[7:0]							
	EQU_CTRL7[15:8]	Reserved[1:0]		Reserved[5:0]					
	EQU_CTRL7[7:0]	Reserved[7:0]							
0xD28	EQU_CTRLA[31:24]	Reserved[1:0]		D1_init[5:0]					
	EQU_CTRLA[23:16]	Reserved	D2_init[6:0]						
	EQU_CTRLA[15:8]	Reserved	D3_init[6:0]						
	EQU_CTRLA[7:0]	Reserved	D4_init[6:0]						
0xD2C	EQU_CTRLB[31:24]	Reserved[1:0]		Reserved[1:0]		capsel[1:0]		Mode6Gphb	Reserved
	EQU_CTRLB[23:16]	Reserved[1:0]		Reserved[5:0]					
	EQU_CTRLB[15:8]	Reserved[7:0]							
	EQU_CTRLB[7:0]	Reserved[7:0]							
0xD3C	EYE_MON2[31:24]	D1ErrChPhPri[7:0]							
	EYE_MON2[23:16]	D1ErrChPhSec[7:0]							
	EYE_MON2[15:8]	Reserved[7:0]							
	EYE_MON2[7:0]	Reserved	Reserved[6:0]						
0xD64	CLK_CTRL1[31:24]	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
	CLK_CTRL1[23:16]	Reserved	Reserved	Reserved	Reserved	Reserved[3:0]			
	CLK_CTRL1[15:8]	Reserved[3:0]				Reserved	cd_tune[2:0]		
	CLK_CTRL1[7:0]	Reserved[3:0]				Reserved	Reserved	Reserved[1:0]	
0xD80	EQU_CTRLD[31:24]	Reserved[1:0]		DFE2_initD3[5:0]					
	EQU_CTRLD[23:16]	Reserved	DFE2_initD2[6:0]						
	EQU_CTRLD[15:8]	Reserved	DFE1_initD3[6:0]						
	EQU_CTRLD[7:0]	Reserved	DFE1_initD2[6:0]						
0xD84	EQU_CTRLE[31:24]	Reserved	DFE4Init_D3[6:0]						
	EQU_CTRLE[23:16]	Reserved	DFE4Init_D2[6:0]						
	EQU_CTRLE[15:8]	Reserved	DFE3Init_D3[6:0]						
	EQU_CTRLE[7:0]	Reserved	DFE3Init_D2[6:0]						
0xD8C	EQU_CTRLG[31:24]	Reserved[7:0]							
	EQU_CTRLG[23:16]	Reserved[7:0]							
	EQU_CTRLG[15:8]	AGCInit_D3[7:0]							
	EQU_CTRLG[7:0]	AGCInit_D2[7:0]							

Register Details

CfgIFA (0x00)

Configure Interface A

BIT	7	6	5	4	3	2	1	0
Field	SftRst	LSBF	AddIncr	Wire4	Wire4_0	AddIncr0	LSBF0	SftRst0
Reset	0b0	0b0	0b0	0b0	0b0	0b0	0b0	0b0
Access Type	Write 1 to Clear, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write 1 to Clear, Read

BITFIELD	BITS	DESCRIPTION	DECODE
SftRst	7	Writing a 1 to this bit resets everything except address 0x0000, 0x0001, and SPI interface. This bit is self-clearing	
LSBF	6	Select MSB-LSB first data format	0x0: MSB first for input control/data and output data 0x1: LSB first for input control/data and output data
AddIncr	5	Configure the auto Increment or Decrement for address in burst mode	0x0: Decrement address for SPI burst mode 0x1: Increment address for SPI burst mode
Wire4	4	Configure 3 or 4 wire SPI mode	0x0: 3-Wire SPI mode, SDIO used for both input and output 0x1: 4-Wire SPI mode, SDIO is input and SDO is output
Wire4_0	3	Same as Bit4 and both should have the same value	
AddIncr0	2	Same as Bit5 and both should have the same value	
LSBF0	1	Same as Bit6 and both should have the same value	
SftRst0	0	Same as Bit7 and both should have the same value	

CfgIFB (0x01)

Configure Interface B

BIT	7	6	5	4	3	2	1	0
Field	StrmDis	rsvd6	–	rsvd4	rsvd3	–	–	rsvd0
Reset	0b0	0b0	–	0b0	0b0	–	–	0b0
Access Type	Write, Read	Write, Read	–	Write, Read	Write, Read	–	–	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
StrmDis	7	Configure the Burst SPI mode	0x0: SPI Streaming mode is enabled 0x1: SPI Streaming mode is disabled and continued CSB forces intruction-data format
rsvd6	6	Reserved Bit	
rsvd4	4	Reserved Bit	
rsvd3	3	Reserved Bit	
rsvd0	0	Reserved Bit	

CfgDev (0x02)

Device Configuration

BIT	7	6	5	4	3	2	1	0
Field	rsvd[4:0]					CDrst	PDM[1:0]	
Reset	0x0					0b0	0x0	
Access Type	Write, Read					Write, Read	Write, Read	

BITFIELD	BITS	DESCRIPTION	DECODE
rsvd	7:3	Reserved Bits	
CDrst	2	Clock Divider Reset	0x0: Clock Divider is not reset 0x1: Clock Divider is reset
PDM	1:0	Power-Down Modes Configuration	0x0: Normal operation mode 0x1: (optional) Low-power, normal operation with reduced power and corresponding performance 0x2: (optional) Medium-power standby mode, non-operational, but return to full operation in minimum amount of time 0x3: Sleep mode with lowest power dissipation with chip inactivity except SPI interface

ChipType (0x03)

Chip Type Status

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	Type[3:0]			
Reset	–	–	–	–	0x4			
Access Type	–	–	–	–	Read Only			

BITFIELD	BITS	DESCRIPTION	DECODE
Type	3:0	Chip Type Status	0x0: Not Assigned 0x1: RF 0x2: IF 0x3: High-speed ADC 0x4: High-speed DAC 0x5: Clock Buffer 0x6: PLL 0x7: Precision ADC 0x8: Precision DAC 0x9: RAD 0xA: Reserved 0xB: Reserved 0xC: Reserved 0xD: Reserved 0xE: Reserved 0xF: Not assigned

ChipID1 (0x04)

Chip ID LSB

BIT	7	6	5	4	3	2	1	0
Field	CIDLSB[1:0]		PID[1:0]		FID[3:0]			
Reset	0x0		0x0		0x0			
Access Type	Read Only		Read Only		Read Only			

BITFIELD	BITS	DESCRIPTION
CIDLSB	7:6	Product Unique Chip ID-2LSB
PID	5:4	Product-Line part of Chip ID
FID	3:0	Functional part of Chip ID

ChipID2 (0x05)

Chip ID MSB

BIT	7	6	5	4	3	2	1	0
Field	CIDMSB[7:0]							
Reset	0x80							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
CIDMSB	7:0	Product Unique Chip ID-8MSB

ChipRev (0x06)

Chip Revision

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	Rev[3:0]			
Reset	–	–	–	–	0x0			
Access Type	–	–	–	–	Read Only			

BITFIELD	BITS	DESCRIPTION
Rev	3:0	Chip Revision ID

VendID1 (0x0C)

Vendor ID LSB

BIT	7	6	5	4	3	2	1	0
Field	VIDLSB[7:0]							
Reset	0x6A							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
VIDLSB	7:0	Vendor ID LSB Byte

VendID2 (0x0D)

Vendor ID MSB

BIT	7	6	5	4	3	2	1	0
Field	VIDMSB[7:0]							
Reset	0x0B							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
VIDMSB	7:0	Vendor ID MSB Byte

CfgDACrate (0x10)

Configure DAC Update Rate

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	Drate[3:0]			
Reset	–	–	–	–	0x5			
Access Type	–	–	–	–	Write, Read			

BITFIELD	BITS	DESCRIPTION	DECODE
Drate	3:0	Configure DAC rate	0x0: 2457.6MHz 0x1: 2949.6MHz 0x2: 3686.4MHz 0x3: 3932.2MHz 0x4: 4423.7MHz 0x5: 4915.2MHz (default) 0x6: 5898.2MHz 0x7: Reserved 0x8: Reserved 0x9: Reserved 0xA: Reserved 0xB: Reserved 0xC: Reserved 0xD: Reserved 0xE: Reserved 0xF: Reserved

CfgCLKrate (0x11)

Configure CLKP/N Input Rate

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	Crate[3:0]			
Reset	–	–	–	–	0xD			
Access Type	–	–	–	–	Write, Read			

BITFIELD	BITS	DESCRIPTION	DECODE
Crate	3:0	CLKP/N rate configuration	0x0: 245.76MHz 0x1: 307.2MHz 0x2: 368.64MHz 0x3: 491.52MHz 0x4: 737.28MHz 0x5: 983.04MHz 0x6: 1228.8MHz 0x7: 1474.56MHz 0x8: 2457.6MHz 0x9: 2949.6MHz 0xA: 3686.4MHz 0xB: 3932.2MHz 0xC: 4423.7MHz 0xD: 4915.2MHz (default) 0xE: 5898.2MHz 0xF: Reserved

CfgREGS (0x12)

Configure Register options

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	–	rsvd	IntCfg
Reset	–	–	–	–	–	–	0b0	0b0
Access Type	–	–	–	–	–	–	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
rsvd	1	Reseverd Bit	
IntCfg	0	Enable the Internal Configuration Mode. GLBL.CfgIFC.xfer triggers the internal configuration process and after it is complete, the DSP.STATUS.TRDY latched status is set. The registers/fields configured are DSP.CfgPLL1 DSP.CfgPLL2 DSP.CfgClkDiv SerDesRegs.CfgSerDes.RxRateSel SerDesRegs.CfgSerDes.PhyWMode CMURegs.CfgfCMU1	0x0: Internal register configuration is disabled 0x1: When CfgIFC.Xfer bit is set, some registers are configured internally.

CfgChipOM (0x100)

Configure Chip Operation Mode

BIT	7	6	5	4	3	2	1	0
Field	–	RclkM[1:0]		INVQ	–	Mute	–	DFMT
Reset	–	0x0		0b0	–	0b1	–	0b0
Access Type	–	Write, Read		Write, Read	–	Write, Read	–	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
RclkM	6:5	RCLK output mode	0x0: DAC clock divided by (interpolation ratio * 1) 0x1: DAC clock divided by (interpolation ratio * 2) 0x2: DAC clock divided by (interpolation ratio * 4) 0x3: DAC clock divided by (interpolation ratio * 4)
INVQ	4	Configure the Q inversion	0x0: Disable DAC I-Q data Q being inverted to make I-Q 0x1: Enable DAC I-Q data Q being inverted to make I+Q
Mute	2	Control DAC mute-unmute mode	0x0: DAC in normal mode 0x1: Put DAC into mute mode
DFMT	0	Configure the DAC interface data format	0x0: DAC Input data in two's complement format 0x1: DAC Input data in offset binary format

CfgDSP (0x101)

Configure DSP engine

BIT	7	6	5	4	3	2	1	0
Field	R[3:0]				RstDSP	RstFIFO	NCOE	NCOLD
Reset	0x0				0b0	0b0	0b0	0b0
Access Type	Write, Read				Write, Read	Write, Read	Write, Read	Write 1 to Set, Read

BITFIELD	BITS	DESCRIPTION	DECODE
R	7:4	Define interpolation ratio	0x0: 4X interpolation 0x1: DSP bypass mode: bypasses interpolators and modulator. 0x2: All undefined values are reserved
RstDSP	3	Reset DSP (Input FIFO, interpolation filters, complex modulator, NCO)	0x0: No Reset 0x1: Reset DSP
RstFIFO	2	Reset input data FIFO	0x0: No Reset 0x1: Reset FIFO
NCOE	1	Enable/Disable Extended NCO mode	0x0: Disable Extended NCO mode for DAC 0x1: Enable Extended NCO mode for 10KHz spacing
NCOLD	0	Writing a 1 loads NCO configuration for DAC. This bit is self clearing.	0x0 0x1: Loads NCO configuration for DAC

CfgNCOF0 (0x102)

Configure NCO Frequency Control Word for DAC DSP, bits[7:0]

BIT	7	6	5	4	3	2	1	0
Field	FCW[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
FCW	7:0	Configure NCO Frequency Control Word for DAC DSP, bits[7:0]

CfgNCOF1 (0x103)

Configure NCO Frequency Control Word for DAC DSP, bits[15:8]

BIT	7	6	5	4	3	2	1	0
Field	FCW[15:8]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
FCW	7:0	Configure NCO Frequency Control Word for DAC DSP, bits[15:8]

CfgNCOF2 (0x104)

Configure NCO Frequency Control Word for DAC DSP, bits[23:16]

BIT	7	6	5	4	3	2	1	0
Field	FCW[23:16]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
FCW	7:0	Configure NCO Frequency Control Word for DAC DSP, bits[23:16]

CfgNCOF3 (0x105)

Configure NCO Frequency Control Word for DAC DSP, bits[31:24]

BIT	7	6	5	4	3	2	1	0
Field	FCW[31:24]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
FCW	7:0	Configure NCO Frequency Control Word for DAC DSP, bits[31:24]

CfgNCON0 (0x106)

Configure NCO Frequency Control Word Numerator Word for DAC DSP, bits[7:0]

BIT	7	6	5	4	3	2	1	0
Field	NFW[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
NFW	7:0	Configure NCO Frequency Control Word Numerator Word for DAC DSP, bits[7:0]

CfgNCON1 (0x107)

Configure NCO Frequency Control Word Numerator Word for DAC DSP, bits[15:8]

BIT	7	6	5	4	3	2	1	0
Field	NFW[15:8]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
NFW	7:0	Configure NCO Frequency Control Word Numerator Word for DAC DSP, bits[15:8]

CfgNCON2 (0x108)

Configure NCO Frequency Control Word Numerator Word for DAC DSP, bits[17:16]

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	–	NFW[17:16]	
Reset	–	–	–	–	–	–	0x0	
Access Type	–	–	–	–	–	–	Write, Read	

BITFIELD	BITS	DESCRIPTION
NFW	1:0	Configure NCO Frequency Control Word Numerator Word for DAC DSP, bits[17:16]

CfgNCOD0 (0x109)

Configure NCO Frequency Control Word Denominator Word for DAC DSP, bits [7:0]

BIT	7	6	5	4	3	2	1	0
Field	DFW[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
DFW	7:0	Configure NCO Frequency Control Word Denominator Word for DAC DSP, bits[7:0]

CfgNCOD1 (0x10A)

Configure NCO Frequency Control Word Denominator Word for DAC DSP, bits [15:8]

BIT	7	6	5	4	3	2	1	0
Field	DFW[15:8]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
DFW	7:0	Configure NCO Frequency Control Word Denominator Word for DAC DSP, bits[15:8]

CfgNCOD2 (0x10B)

Configure NCO Frequency Control Word Denominator Word for DAC DSP, bits [18:16]

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	DFW[18:16]		
Reset	–	–	–	–	–	0x0		
Access Type	–	–	–	–	–	Write, Read		

BITFIELD	BITS	DESCRIPTION
DFW	2:0	Configure NCO Frequency Control Word Denominator Word for DAC DSP, bits[18:16]

CfgNCOU (0x10C)

Configure NCO Update for DAC DSP

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	–	RLM[1:0]	
Reset	–	–	–	–	–	–	0x0	
Access Type	–	–	–	–	–	–	Write, Read	

BITFIELD	BITS	DESCRIPTION	DECODE
RLM	1:0	NCO Frequency Control Word update mode	0x0: Load immediately with no glitch control 0x2: Use step increment/decrement mode for loading

CfgNCOUT0 (0x10D)

Configure NCO Update Timer for DAC DSP, bit[7:0]

BIT	7	6	5	4	3	2	1	0
Field	TIM[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
TIM	7:0	NCO Update Timer value in NCO clock cycles (x8) before NCO update is forced

CfgNCOUT1 (0x10E)

Configure NCO Update Timer for DAC DSP, bits[15:8]

BIT	7	6	5	4	3	2	1	0
Field	TIM[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
TIM	7:0	NCO Update Timer value in NCO clock cycles (x8) before NCO update is forced

CfgNCOUT2 (0x10F)

Configure NCO Update Timer for DAC DSP, bits[23:16]

BIT	7	6	5	4	3	2	1	0
Field	TIM[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
TIM	7:0	NCO Update Timer value in NCO clock cycles (x8) before NCO update is forced

CfgPM (0x110)

Configure Power Monitor for DAC DSP

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	Start	Mode	Reset
Reset	–	–	–	–	–	0b0	0b0	0b0
Access Type	–	–	–	–	–	Write, Read	Write, Read	Write 1 to Set, Read

BITFIELD	BITS	DESCRIPTION	DECODE
Start	2	Power Monitor Start	
Mode	1	Power Monitor Mode	0x0: Count samples below the threshold 0x1: Count samples above the threshold
Reset	0	Writing a 1 resets the power monitor count. This bit is self-clearing.	0x0 0x1: Resets the power monitor count.

CfgPMT (0x111)

Configure Power Monitor Threshold for DAC DSP

BIT	7	6	5	4	3	2	1	0
Field	PMT[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
PMT	7:0	Configure Power Monitor Threshold value

CfgPMIC0 (0x112)

Configure Power Monitor Init Count 6 x 8 = 48 bits for DAC DSP, bits[7:0]

BIT	7	6	5	4	3	2	1	0
Field	PMIC[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
PMIC	7:0	Count value bits[7:0]

CfgPMIC1 (0x113)

Configure Power Monitor Init Count 6 x 8 = 48 bits for DAC DSP

BIT	7	6	5	4	3	2	1	0
Field	PMIC[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
PMIC	7:0	Count value bits[15:8]

CfgPMIC2 (0x114)

Configure Power Monitor Init Count 6 x 8 = 48 bits for DAC DSP

BIT	7	6	5	4	3	2	1	0
Field	PMIC[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
PMIC	7:0	Count value bits[23:16]

CfgPMIC3 (0x115)

Configure Power Monitor Init Count 6 x 8 = 48 bits for DAC DSP

BIT	7	6	5	4	3	2	1	0
Field	PMIC[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
PMIC	7:0	Count value bits[31:24]

CfgPMIC4 (0x116)

Configure Power Monitor Init Count 6 x 8 = 48 bits for DAC DSP

BIT	7	6	5	4	3	2	1	0
Field	PMIC[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
PMIC	7:0	Count value bits[39:32]

CfgPMIC5 (0x117)

Configure Power Monitor Init Count 6 x 8 = 48 bits for DAC DSP, bits[47:40]

BIT	7	6	5	4	3	2	1	0
Field	PMIC[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
PMIC	7:0	Count value bits[47:40]

StatPM0 (0x118)

Power Monitor Status for DAC DSP

BIT	7	6	5	4	3	2	1	0
Field	PMST[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
PMST	7:0	Power Monitor Status indicating the threshold crossing count, bits[7:0]

StatPM1 (0x119)

Power Monitor Status for DAC DSP

BIT	7	6	5	4	3	2	1	0
Field	PMDONE	–	–	–	PMST[3:0]			
Reset	0b0	–	–	–	0x0			
Access Type	Read Only	–	–	–	Read Only			

BITFIELD	BITS	DESCRIPTION	DECODE
PMDONE	7	Power Monitor Status	0x0: Power Monitor Status update: In Progress 0x1: Power Monitor Status update: Done
PMST	3:0	Power Monitor Status for DAC DSP, bits[11:8]	

CfgSync (0x15A)

Configure multiple-DAC synchronization for DAC DSP

BIT	7	6	5	4	3	2	1	0
Field	–	ClkDiv_ Sync	–	–	–	–	–	–
Reset	–	0b0	–	–	–	–	–	–
Access Type	–	Write, Read	–	–	–	–	–	–

BITFIELD	BITS	DESCRIPTION	DECODE
ClkDiv_Sync	6	Enable/Disable reset to the Clock Divider Block	0x0: Disable reset to the Clock Divider Block 0x1: Enable reset to the Clock Divider Block

CfgFIFO (0x15B)

Configure Input FIFO for DAC

BIT	7	6	5	4	3	2	1	0
Field	rsvd[4:0]					DupI	SwapIQ	RevBitOrd
Reset	0x0							
Access Type	Write, Read					Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
rsvd	7:3	Reserved Bits	
DupI	2	Duplicate I data in the input FIFO for DAC	0x0: Do not duplicate I 0x1: Duplicate I
SwapIQ	1	Reverse I/Q Order in the input FIFO for DAC	0x0: Normal I/Q Order 0x1: Reverse I/Q Order
RevBitOrd	0	Reverse LSB/MSB Order in the input FIFO for DAC	0x0: Normal LSB/MSB Order 0x1: Reverse LSB/MSB Order

CfgRSV0 (0x15D)

Configure Reserved, bits[7:0]

BIT	7	6	5	4	3	2	1	0
Field	RSV[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
RSV	7:0	Reserved

CfgRSV1 (0x15E)

Configure Reserved, bits[15:8]

BIT	7	6	5	4	3	2	1	0
Field	RSV[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
RSV	7:0	Reserved

CfgRSV2 (0x15F)

Configure Reserved, bits[23:16]

BIT	7	6	5	4	3	2	1	0
Field	RSV[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
RSV	7:0	Reserved

CfgRSV3 (0x160)

Configure Reserved, bits[31:24]

BIT	7	6	5	4	3	2	1	0
Field	RSV[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
RSV	7:0	Reserved

EMUTE (0x162)

Mute Enable Register for DAC

BIT	7	6	5	4	3	2	1	0
Field	EM[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
EM	7:0	Enable/Disable Mute bit 0-7 in register STATUS	0x0: Disable Mute bit 0-7 in register STATUS 0x1: Enable Mute bit 0-7 in register STATUS

EINT (0x163)

Interrupt Enable Register for DAC DSP

BIT	7	6	5	4	3	2	1	0
Field	INT_EN[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
INT_EN	7:0	Enable/Disable interrupt bit 0-7 in register STATUS	0x0: Disable interrupt bit 0-7 in register STATUS 0x1: Enable interrupt bit 0-7 in register STATUS

STATUS (0x164)

Status Register for DAC DSP

BIT	7	6	5	4	3	2	1	0
Field	JSDIM	JSDII	rsvd[2:0]			TRDY	–	PLLlck
Reset							–	
Access Type	Read Only	Read Only	Read Only			Write 0 to Clear, Read	–	Write 0 to Clear, Read

BITFIELD	BITS	DESCRIPTION	DECODE
JSDIM	7	JSDI Link layer Mute active/inactive status	0x0: Indicates JSDI Link layer Mute is not active 0x1: Indicates JSDI Link layer Mute is active
JSDII	6	JSDI Link layer Interrupt active/inactive status	0x0: Indicates JSDI Link layer Interrupt is not active 0x1: Indicates JSDI Link layer Interrupt is active
rsvd	5:3	Reserved Bits	
TRDY	2	Trim loading complete or internal configuration complete, latched status	0x0: Trim loading is in progress 0x1: Trim loading complete after RESETB deassertion, latched status Internal Configuration complete after setting GLB.CfgIFC.Xfer, latched status
PLLlck	0	DAC PLL loss-of-lock, latched status	0x0: DAC PLL locked 0x1: DAC PLL loss-of-lock, latched status

RSVD7 (0x165)

Reserved Address Space

BIT	7	6	5	4	3	2	1	0
Field	rsvd[7:0]							
Reset								
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
rsvd	7:0	

DEVSN0 (0x166)

MAX5857 RF DAC Serial Number, bits[7:0]

BIT	7	6	5	4	3	2	1	0
Field	SN[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
SN	7:0	MAX5857 RF DAC Serial Number, bits[7:0]

DEVSN1 (0x167)

MAX5857 RF DAC Serial Number, bits[15:8]DEVSN2 (0x168)

MAX5857 RF DAC Serial Number, bits[23:16]CfgPLL0 (0x180)

Configure DAC PLL, bits[7:0]

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	–	–	MASTER
Reset	–	–	–	–	–	–	–	0b0
Access Type	–	–	–	–	–	–	–	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
MASTER	0	MASTER: 1V digital control logic input (active-low) that resets counter clock (div-by-4096), edge detector, and counter = 000000.	0x0 0x1: Force restart PLL digital tuning by toggling from 1 to 0 and back to 1

CfgPLL1 (0x181)

Configure DAC PLL, bits[15:8]

BIT	7	6	5	4	3	2	1	0
Field	–	PLL_BYP	DVAL0[1:0]		PVAL	RVAL0	–	–
Reset	–	0b1	0x0		0b0	0b0	–	–
Access Type	–	Write, Read	Write, Read		Write, Read	Write, Read	–	–

BITFIELD	BITS	DESCRIPTION			DECODE
PLL_BYP	6	PLL_BYP: 1V digital control logic input set to "1" to power down the entire PLL.			0x0 0x1: Power down the entire PLL
DVAL0	5:4	DVAL<1:0>: 1V digital control logic input to control feedback FB divider. See table below for DVAL[3:0] values.			
		VALUE	**ENUMERATION**	**DECODE**	
		0x0		16	
		0x1		20	
		0x2		24	
		0x3		28	
		0x4		16	
		0x5		20	
		0x6		24	
		0x7		28	
		0x8		32	
		0x9		36	
		0xA		40	
		0xB		44	
		0xC		48	
		0xD		52	
		0xE		56	
		0xF		60	
PVAL	3	PVAL: 1V digital control logic input to control output divider.			0x0: div-by-2 0x1: div-by-1 (bypass mode)
RVAL0	2	RVAL<0>: 1V digital control logic input to control reference divider. RVAL<1:0> table shows below			
		VALUE	**ENUMERATION**	**DECODE**	
		0x0		div-by-8	
		0x1		div-by-4	
		0x2		div-by-2	
		0x3		div-by-1 (bypass mode)	

CfgPLL2 (0x182)

Configure DAC PLL, bits[23:16]

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	DVAL1[1:0]		RVAL1	–	VCO_SEL
Reset	–	–	–	0x0		0b0	–	0b0
Access Type	–	–	–	Write, Read		Write, Read	–	Write, Read

BITFIELD	BITS	DESCRIPTION			DECODE
DVAL1	4:3	DVAL<3:2>. See below for DVAL[3:0] table			
		VALUE	**ENUMERATION**	**DECODE**	
		0x0		16	
		0x1		20	
		0x2		24	
		0x3		28	
		0x4		16	
		0x5		20	
		0x6		24	
		0x7		28	
		0x8		32	
		0x9		36	
		0xA		40	
		0xB		44	
		0xC		48	
		0xD		52	
		0xE		56	
		0xF		60	
RVAL1	2	RVAL<1>: 1V digital control logic input to control reference divider. RVAL<1:0> table shows below			
		VALUE	**ENUMERATION**	**DECODE**	
		0x0		div-by-8	
		0x1		div-by-4	
		0x2		div-by-2	
		0x3		div-by-1 (bypass mode)	
VCO_SEL	0	VCO_SEL: 1V digital control logic input to select high-band or low-band VCO core. Logic "0" selects the low-band VCO, logic "1" selects the high-band VCO.			0x0: Selects the low-band VCO 0x1: Selects the high-band VCO

StatPLL0 (0x183)

DAC PLL Status, bits[7:0]

BIT	7	6	5	4	3	2	1	0
Field	rsvd[3:0]				PLL_LOCK	–	–	–
Reset						–	–	–
Access Type	Read Only				Read Only	–	–	–

BITFIELD	BITS	DESCRIPTION	DECODE
rsvd	7:4	Reserved Bits	
PLL_LOCK	3	PLL lock detect	0x0: PLL not locked 0x1: PLL locked

CfgClkDiv (0x185)

Clock Generator Output Divider

BIT	7	6	5	4	3	2	1	0
Field	RDIV[3:0]				RSV[1:0]		PCLK[1:0]	
Reset	0x6				0x0		0x0	
Access Type	Write, Read				Write, Read		Write, Read	

BITFIELD	BITS	DESCRIPTION	DECODE
RDIV	7:4	Clock divider setting for RCLKi. RCLKi is set to Internal DAC Clock rate divided by the RDIV3:0 setting. RCLKi drives the input of the following RCLK (CfgChipOM.RclkM1-0) and CMU (CfgCMU1.Cref_divsel1p0) dividers.	0x0: Off 0x1: Divide by 4 0x2: Divide by 5 0x3: Divide by 6 0x4: Divide by 8 0x5: Divide by 10 0x6: Divide by 12 0x7: Divide by 16 0x8: Divide by 20 0x9: Divide by 24 0xA: Reserved 0xB: Reserved 0xC: Reserved 0xD: Reserved 0xE: Reserved 0xF: Reserved
RSV	3:2	Reserved Bits	
PCLK	1:0	Divide ratio for PCLK used by the APB bus in the RxLink Layer	0x1: RCLK 0x2: DAC clock by 16 0x3: DAC clock by 8

CfgRLinkSet (0x400)

Configure Rx Link Settings

BIT	31	30	29	28	27	26	25	24
Field	–	–	–	–	–	–	–	–
Reset	–	–	–	–	–	–	–	–
Access Type	–	–	–	–	–	–	–	–
Bit	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Field	–	–	–	–	–	–	SyncInit	SyncPol
Reset	–	–	–	–	–	–	0x0	0x0
Access Type	–	–	–	–	–	–	Write, Read	Write, Read
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**
Field	–	–	–	–	–	–	IgnDisp	ScrmD
Reset	–	–	–	–	–	–	0x0	0x0
Access Type	–	–	–	–	–	–	Write, Read	Write, Read
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Field	–	–	DDiv[1:0]		Subclass[1:0]		RstSRL	RstILA
Reset	–	–	0x0		0x0		0x0	0x0
Access Type	–	–	Write, Read		Write, Read		Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
SyncInit	17	Out-of-reset value for SYNC~	0: RxLink SYNC~ initial value is 0 1: RxLink SYNC~ initial value is 1
SyncPol	16	SYNCN polarity control	0: RxLink SYNC~ error reporting is active-low, which includes both resynchronization request and error reporting; normal state is high and resync request/error state is low per JESD204B standard 1: RxLink SYNC~ error reporting is active-high, which includes both resynchronization request and error reporting; normal state is low and resync request/error state is high
IgnDisp	9	Running Disparity errors ignore for data processing control	0: Running Disparity errors are not ignored 1: Running Disparity errors are ignored
ScrmD	8	Descrambler disable control	0: Descrambling is enabled 1: Descrambling is disabled
DDiv	5:4	Device Clock to Frame Clock ratio select	0: Device Clock to Frame Clock ratio is 1 1: Device Clock to Frame Clock ratio is 2 2: Device Clock to Frame Clock ratio is 4 3: Device Clock to Frame Clock ratio is 8

BITFIELD	BITS	DESCRIPTION	DECODE
Subclass	3:2	JESD204B subclass	0: Subclass 0 1: Subclass 1 (Not supported) 2: Subclass 2 (Not supported) 3: Reserved
RstSRL	1	Soft Reset to clear all Status Registers Latched, active high	0: Latched statuses are not cleared 1: Latched statuses are cleared
RstILA	0	Soft Reset for ILA engine, active high	0: ILA engine is not reset 1: ILA engine is reset

CfgRLinkParam1 (0x404)

Configure Link for parameters M, L, F and S

BIT	31	30	29	28	27	26	25	24
Field	–	–	–	CfgS[4:0]				
Reset	–	–	–	0x0				
Access Type	–	–	–	Write, Read				
Bit	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Field	CfgF[7:0]							
Reset	0x0							
Access Type	Write, Read							
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**
Field	–	–	–	CfgL[4:0]				
Reset	–	–	–	0x0				
Access Type	–	–	–	Write, Read				
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Field	CfgM[7:0]							
Reset	0x0							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
CfgS	28:24	Number of samples per frame is (CfgS+1)
CfgF	23:16	Number of octets per frame is (CfgF+1)
CfgL	12:8	Number of active lanes in the Link is (CfgL+1)
CfgM	7:0	Number of active converters in the Link is (CfgM+1)

CfgRLinkParam2 (0x408)

Configure Link for parameter K and ILA sequence configuration

BIT	31	30	29	28	27	26	25	24
Field	DID[7:0]							
Reset	0x0							
Access Type	Write, Read							
Bit	23	22	21	20	19	18	17	16
Field	HD	–	–	–	BID[3:0]			
Reset	0x0	–	–	–	0x0			
Access Type	Write, Read	–	–	–	Write, Read			
Bit	15	14	13	12	11	10	9	8
Field	CfgNP[2:0]			CfgN[4:0]				
Reset	0x0			0x00				
Access Type	Write, Read			Write, Read				
Bit	7	6	5	4	3	2	1	0
Field	–	–	–	CfgK[4:0]				
Reset	–	–	–	0x0				
Access Type	–	–	–	Write, Read				

BITFIELD	BITS	DESCRIPTION
DID	31:24	Device ID used for ILA sequence checking
HD	23	HD bit used for ILA sequence checking
BID	19:16	Bank ID used for ILA sequence checking
CfgNP	15:13	Number of bits per sample rounded up to nibble groups is (CfgNP+1)*4
CfgN	12:8	Number of bits per sample is (CfgN+1)
CfgK	4:0	Number of frames per multiframe is (CfgK+1)

CfgRLinkCtrl (0x410)

Configure Rx Link Control

BIT	31	30	29	28	27	26	25	24
Field	–	–	–	–	–	–	–	–
Reset	–	–	–	–	–	–	–	–
Access Type	–	–	–	–	–	–	–	–
Bit	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Field	–	SCtrl[1:0]		DFSync	–	–	–	–
Reset	–	0x0		0x0	–	–	–	–
Access Type	–	Write, Read		Write, Read	–	–	–	–
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**
Field	–	–	–	–	–	–	–	SErrC
Reset	–	–	–	–	–	–	–	0x0
Access Type	–	–	–	–	–	–	–	Write, Read
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Field	–	–	–	–	BitSwap	–	AsyncAvl	rclk
Reset	–	–	–	–	0x0	–	0x0	0x1
Access Type	–	–	–	–	Write, Read	–	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
SCtrl	22:21	ILA sequence detection control	0: ILA sequence detection is enabled 1: ILA sequence detection is disabled for the first CfgRLinkMFrame.SNum frames 2: ILA sequence detection is disabled
DFSync	20	ILA restart on frame resynchronization control	0: Enable ILA restart on frame resynchronization 1: Disable ILA restart on frame resynchronization
SErrC	8	SYNC~ assert/deassert cycle control	0: SYNC~ error reporting assertion/deassertion per JESD204B 1: Enable SYNC~ error reporting assertion/deassertion on any frame - JESD204A
BitSwap	3	Bit Swap control	0: Disable Bit Swap MSB<->LSB within an octet of the Lane data 1: Enable Bit Swap MSB<->LSB within an octet of the Lane data
AsyncAvl	1	Initial Frame Synchronization state machine control	0: Intial Frame Synchronization state machine includes the FS_CHECK state 1: Intial Frame Synchronization state machine bypasses the FS_CHECK state
rclk	0	Frame/sample clock source	0: Divided down Device Clock is used as frame/sample clock 1: Frame clock input from DAC/DSP is used as frame/sample clock when the Device Clock is not available

CfgRLinkMFrame (0x414)

Configure Multiframe control

BIT	31	30	29	28	27	26	25	24
Field	–	–	–	–	–	–	SNum[8:7]	
Reset	–	–	–	–	–	–	0x3	
Access Type	–	–	–	–	–	–	Write, Read	
Bit	23	22	21	20	19	18	17	16
Field	SNum[6:0]							MFSel[8]
Reset	0x3							0x4
Access Type	Write, Read							Write, Read
Bit	15	14	13	12	11	10	9	8
Field	MFSel[7:0]							
Reset	0x4							
Access Type	Write, Read							
Bit	7	6	5	4	3	2	1	0
Field	–	–	ILADly[5:0]					
Reset	–	–	0x0					
Access Type	–	–	Write, Read					

BITFIELD	BITS	DESCRIPTION
SNum	25:17	ILA sequence number of multiframes
MFSel	16:8	ILA multiframe count for FIFO write start
ILADly	5:0	ILA Delay frame clock count for FIFO read start, ILADly configuration sets the FIFO read start time relative to the multiframe boundary, for a desired FIFO depth possibly to minimize latency

CfgRSYNCN (0x418)

SYNC~ Error Reporting control

BIT	31	30	29	28	27	26	25	24
Field	–	–	–	–	–	–	–	–
Reset	–	–	–	–	–	–	–	–
Access Type	–	–	–	–	–	–	–	–
Bit	23	22	21	20	19	18	17	16
Field	–	–	–	–	–	–	–	–
Reset	–	–	–	–	–	–	–	–
Access Type	–	–	–	–	–	–	–	–

Bit	15	14	13	12	11	10	9	8
Field	–	RepErr14	RepErr13	RepErr12	RepErr11	RepErr10	RepErr9	RepErr8
Reset	–	0x0	0x0	0x0	0x0	0x0	0x0	0x0
Access Type	–	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read
Bit	7	6	5	4	3	2	1	0
Field	–	RepErr6	RepErr5	–	–	RepErr2	RepErr1	RepErr0
Reset	–	0x0	0x0	–	–	0x0	0x0	0x0
Access Type	–	Write, Read	Write, Read	–	–	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
RepErr14	14	ILA Fail error control for Error Reporting, only if JESD204B-TX needs to monitor the RxLink errors	0: ILA Fail error is disabled 1: ILA Fail error is enabled
RepErr13	13	Reserved	
RepErr12	12	FIFO empty error control for Error Reporting	0: FIFO empty error is disabled 1: FIFO empty error is enabled
RepErr11	11	FIFO full error control for Error Reporting	0: FIFO full error is disabled 1: FIFO full error is enabled
RepErr10	10	Lane Configuration in ILA sequence FCS check error control for Error Reporting	0: Lane Configuration in ILA sequence FCS check error is disabled 1: Lane Configuration in ILA sequence FCS check error is enabled
RepErr9	9	Lane Configuration in ILA sequence mismatch error control for Error Reporting, This is corresponding to the StatRLane.LCfgErr status	0: Lane Configuration in ILA sequence mismatch error is disabled 1: Lane Configuration in ILA sequence mismatch error is enabled
RepErr8	8	ILA sequence control character error control for Error Reporting, This is corresponding to the StatRLane.ILAerr status	0: ILA sequence control character error is disabled 1: ILA sequence control character error is enabled
RepErr6	6	Lane realignment event control for Error Reporting	0: Lane realignment event is disabled 1: Lane realignment event is enabled
RepErr5	5	Frame realignment event control for Error Reporting	0: Frame realignment event is disabled 1: Frame realignment event is enabled
RepErr2	2	8b10b Running Disparity error control for Error Reporting	0: 8b10b Running Disparity error is disabled 1: 8b10b Running Disparity error is enabled
RepErr1	1	8b10b NIT error control for Error Reporting	0: 8b10b Not-in-table error is disabled 1: 8b10b Not-in-table error is enabled
RepErr0	0	Reserved	

CfgRFIFO (0x41C)

Configure Rx Lane FIFOs

BIT	31	30	29	28	27	26	25	24
Field	–	–	–	–	–	–	–	–
Reset	–	–	–	–	–	–	–	–
Access Type	–	–	–	–	–	–	–	–
Bit	23	22	21	20	19	18	17	16
Field	–	–	–	–	–	–	–	–
Reset	–	–	–	–	–	–	–	–
Access Type	–	–	–	–	–	–	–	–
Bit	15	14	13	12	11	10	9	8
Field	–	–	–	MaxFD[4:0]				
Reset	–	–	–	0x1A				
Access Type	–	–	–	Write, Read				
Bit	7	6	5	4	3	2	1	0
Field	–	–	–	MinFD[4:0]				
Reset	–	–	–	0x6				
Access Type	–	–	–	Write, Read				

BITFIELD	BITS	DESCRIPTION
MaxFD	12:8	Maximum FIFO depth for FIFO full status, The FIFO full latched status is indicated if the Lane FIFO depth ever increases beyond this configuration; This field should be set at least CfgF+1 away from the maximum of 32 with some additional margin for clock domain crossing. The default value of 26 (1Ah) should work for all the modes
MinFD	4:0	Minimum FIFO depth for FIFO empty status, The FIFO empty latched status is indicated if the Lane FIFO depth ever decreases below this configuration; This field should be set at least CfgF+1 away from the minimum of 0 with some additional margin for clock domain crossing; The default value of 6 (06h) should work for all the modes

CfgRTestCtrl (0x420)

Configure Rx Link Test feature control

BIT	31	30	29	28	27	26	25	24
Field	–	–	–	–	–	–	–	LnCntType-Sel[3]
Reset	–	–	–	–	–	–	–	0x0
Access Type	–	–	–	–	–	–	–	Write, Read
Bit	23	22	21	20	19	18	17	16
Field	LnCntTypeSel[2:0]			RxCntLaneSel[4:0]				
Reset	0x0			0x0				
Access Type	Write, Read			Write, Read				
Bit	15	14	13	12	11	10	9	8
Field	–	–	SamLoad	RxLoad	CDcorEn	Rsvd0	–	–
Reset	–	–	0x0	0x0	0x0	0x0	–	–
Access Type	–	–	Write 1 to Toggle, Read	Write 1 to Toggle, Read	Write, Read	Write, Read	–	–
Bit	7	6	5	4	3	2	1	0
Field	–	–	–	PRBStype[1:0]		–	RxPRBSen	SamPRB-S15En
Reset	–	–	–	0x0		–	0x0	0x0
Access Type	–	–	–	Write, Read		–	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
LnCntTypeSel	24:21	Lane debug counter error type select	0: No counts, counter disabled 1: NIT errors 2: Running Disparity errors 3: /K/ detect count 4: /R/ detect count 5: /Q/ detect count 6: /A/ detect count 7: /F/ detect count 8: Unexpected control character count for unknown control character outside /K/, /A/, /F/, /R/ and /Q/ is detected 9: ILA sequence control character error count corresponding to the StatRLane.ILAerr bit
RxCntLaneSel	20:16	Invalid character counter Lane select for CntRLaneInvld	

BITFIELD	BITS	DESCRIPTION	DECODE
SamLoad	13	Pulse generation for sample clock domain counter/status update when set to 1, read value should be ignored, This bit is used to load the Lane FIFO depths FIFODepth in the StatRLane registers	
RxLoad	12	Pulse generation for Rx SerDes clock domain counter/status update when set to 1, read value should be ignored, This bit is used to load the Lane debug counter values InvCnt in CntRLaneInvld and DbgCnt in CntRLaneDbg	
CDcorEn	11	Counter clear control	0: Counter data clear-on-read disable 1: Counter data clear-on-read enable
Rsvd0	10	Rsvd0	
PRBStype	4:3	PRBS type for SerDes PHY interface	0: PRBS7 for SerDes Interface when enabled 1: PRBS23 for SerDes Interface when enabled 2: PRBS31 for SerDes Interface when enabled
RxPRBSen	1	Rx PRBS control for SerDes PHY interface	0: Disable PRBS checking on receive SerDes interface 1: Enable PRBS checking on receive SerDes interface, pattern based on PRBStype[1:0]. This bit should be toggled 0->1 to load the incoming data before starting error detection
SamPRB-S15En	0	Sample interface PRBS15 checker control, PRBS checker enabled one sample per frame at a time	0: Disable PRBS15 checker on sample data for all converters 1: Enable PRBS15 checker on sample data for all converters, to be toggled 0->1 to initialize and start the checker

CfgRLinkSTP1 (0x424)

Configure Rx Link Converter Short Test Pattern 1

BIT	31	30	29	28	27	26	25	24
Field	–	–	–	–	–	–	–	–
Reset	–	–	–	–	–	–	–	–
Access Type	–	–	–	–	–	–	–	–
Bit	23	22	21	20	19	18	17	16
Field	–	–	–	–	–	–	–	–
Reset	–	–	–	–	–	–	–	–
Access Type	–	–	–	–	–	–	–	–
Bit	15	14	13	12	11	10	9	8
Field	Sample1[15:8]							
Reset	0x0							
Access Type	Write, Read							
Bit	7	6	5	4	3	2	1	0
Field	Sample1[7:0]							
Reset	0x0							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
Sample1	15:0	Sample 1 of alternating sample Short Test Pattern

CfgRLinkSTP2 (0x428)

Configure Rx Link Converter Short Test Pattern 2

BIT	31	30	29	28	27	26	25	24
Field	–	–	–	–	–	–	–	–
Reset	–	–	–	–	–	–	–	–
Access Type	–	–	–	–	–	–	–	–
Bit	23	22	21	20	19	18	17	16
Field	–	–	–	–	–	–	–	–
Reset	–	–	–	–	–	–	–	–
Access Type	–	–	–	–	–	–	–	–
Bit	15	14	13	12	11	10	9	8
Field	Sample2[15:8]							
Reset	0x0							
Access Type	Write, Read							
Bit	7	6	5	4	3	2	1	0
Field	Sample2[7:0]							
Reset	0x0							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
Sample2	15:0	Sample 2 of alternating sample Short Test Pattern

CfgRLinkIntEn (0x430)

Configure Rx Link Interrupt Enables

BIT	31	30	29	28	27	26	25	24
Field	–	–	–	–	–	–	–	–
Reset	–	–	–	–	–	–	–	–
Access Type	–	–	–	–	–	–	–	–
Bit	23	22	21	20	19	18	17	16
Field	–	–	–	–	–	–	–	–
Reset	–	–	–	–	–	–	–	–
Access Type	–	–	–	–	–	–	–	–
Bit	15	14	13	12	11	10	9	8
Field	–	–	–	–	–	–	–	–
Reset	–	–	–	–	–	–	–	–
Access Type	–	–	–	–	–	–	–	–
Bit	7	6	5	4	3	2	1	0
Field	–	–	–	–	ILAnsync	–	–	ILAfail
Reset	–	–	–	–	0x0	–	–	0x0
Access Type	–	–	–	–	Write, Read	–	–	Write, Read

BITFIELD	BITS	DESCRIPTION
ILAnsync	3	Enable Interrupt on ILA synchronization not achieved real-time
ILAfail	0	Enable Interrupt on ILA failure latched

CfgRLinkMuteEn (0x434)

Configure Rx Link DAC Mute Enables

BIT	31	30	29	28	27	26	25	24
Field	–	–	–	–	–	–	–	–
Reset	–	–	–	–	–	–	–	–
Access Type	–	–	–	–	–	–	–	–
Bit	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Field	–	–	–	–	–	–	–	–
Reset	–	–	–	–	–	–	–	–
Access Type	–	–	–	–	–	–	–	–
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**
Field	–	–	–	–	–	–	–	–
Reset	–	–	–	–	–	–	–	–
Access Type	–	–	–	–	–	–	–	–
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Field	–	–	–	–	ILAnsync	–	–	ILAfail
Reset	–	–	–	–	0x0	–	–	0x0
Access Type	–	–	–	–	Write, Read	–	–	Write, Read

BITFIELD	BITS	DESCRIPTION
ILAnsync	3	Enable Mute on ILA synchronization not achieved real-time
ILAfail	0	Enable Mute on ILA failure latched

StatRLinkILA (0x438)

RxLink ILA engine latched statuses

BIT	31	30	29	28	27	26	25	24
Field	–	–	–	–	–	–	–	–
Reset	–	–	–	–	–	–	–	–
Access Type	–	–	–	–	–	–	–	–
Bit	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Field	–	–	–	–	–	–	–	–
Reset	–	–	–	–	–	–	–	–
Access Type	–	–	–	–	–	–	–	–
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**
Field	–	–	–	–	–	–	–	–
Reset	–	–	–	–	–	–	–	–
Access Type	–	–	–	–	–	–	–	–
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Field	–	–	–	–	ILAnsync	–	–	ILAfailure
Reset	–	–	–	–	0x0	–	–	0x0
Access Type	–	–	–	–	Read Only	–	–	Write 0 to Clear, Read

BITFIELD	BITS	DESCRIPTION
ILAnsync	3	ILA synchronization not achieved status, real-time, indicating that the Lane FIFO writes did not start for the lanes enabled for Initial Lane Alignment process through the CfgRLaneSet.LkSel configuration
ILAfailure	0	ILA failure latched status, indicating that at least one of the Lane FIFOs overflowed before the FIFO reads started waiting for ILA DELAY set with CfgRLinkMFrame.ILADly during the Initial Lane Alignment process or if FIFO writes did not start on a Lane that is not included in the Initial Lane Alignment process through the CfgRLaneSet.LkSel configuration

StatRLinkSTP (0x43C)

Rx Link Sample Interface Short Test Pattern checker status

BIT	31	30	29	28	27	26	25	24
Field	–	–	–	–	–	–	–	–
Reset	–	–	–	–	–	–	–	–
Access Type	–	–	–	–	–	–	–	–
Bit	23	22	21	20	19	18	17	16
Field	–	–	–	–	–	–	–	–
Reset	–	–	–	–	–	–	–	–
Access Type	–	–	–	–	–	–	–	–
Bit	15	14	13	12	11	10	9	8
Field	–	–	–	–	–	–	–	–
Reset	–	–	–	–	–	–	–	–
Access Type	–	–	–	–	–	–	–	–
Bit	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	–	STPerr1	STPerr0
Reset	–	–	–	–	–	–	0x0	0x0
Access Type	–	–	–	–	–	–	Write 0 to Clear, Read	Write 0 to Clear, Read

BITFIELD	BITS	DESCRIPTION
STPerr1	1	STP error for each converter status latched
STPerr0	0	STP error for each converter status latched

StatRLinkPRBS (0x440)

Rx Link Sample Interface PRBS15 checker status

BIT	31	30	29	28	27	26	25	24
Field	–	–	–	–	–	–	–	–
Reset	–	–	–	–	–	–	–	–
Access Type	–	–	–	–	–	–	–	–
Bit	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Field	–	–	–	–	–	–	–	–
Reset	–	–	–	–	–	–	–	–
Access Type	–	–	–	–	–	–	–	–
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**
Field	–	–	–	–	–	–	–	–
Reset	–	–	–	–	–	–	–	–
Access Type	–	–	–	–	–	–	–	–
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Field	–	–	–	–	–	–	PRBSerr1	PRBSerr0
Reset	–	–	–	–	–	–	0x0	0x0
Access Type	–	–	–	–	–	–	Write 0 to Clear, Read	Write 0 to Clear, Read

BITFIELD	BITS	DESCRIPTION
PRBSerr1	1	PRBS error for each converter status latched
PRBSerr0	0	PRBS error for each converter status latched

CntRLaneInvld (0x460)

Rx Lane Counter for 8b10b Invalid errors

BIT	31	30	29	28	27	26	25	24
Field	–	–	–	–	–	–	–	–
Reset	–	–	–	–	–	–	–	–
Access Type	–	–	–	–	–	–	–	–
Bit	23	22	21	20	19	18	17	16
Field	–	–	–	–	–	–	–	–
Reset	–	–	–	–	–	–	–	–
Access Type	–	–	–	–	–	–	–	–
Bit	15	14	13	12	11	10	9	8
Field	InvCnt[15:8]							
Reset	0x0							
Access Type	Read Only							
Bit	7	6	5	4	3	2	1	0
Field	InvCnt[7:0]							
Reset	0x0							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
InvCnt	15:0	Invalid character count for lane # controlled by CfgRTestCtrl.RxCntLaneSel, loaded on setting CfgRTestCtrl.RxLoad to 1. Invalid characters include NIT and Disparity errors.

CntRLaneDbg (0x464)

Rx Lane Counter for Debug

BIT	31	30	29	28	27	26	25	24
Field	–	–	–	–	–	–	–	–
Reset	–	–	–	–	–	–	–	–
Access Type	–	–	–	–	–	–	–	–
Bit	23	22	21	20	19	18	17	16
Field	–	–	–	–	–	–	–	–
Reset	–	–	–	–	–	–	–	–
Access Type	–	–	–	–	–	–	–	–
Bit	15	14	13	12	11	10	9	8
Field	DbgCnt[15:8]							
Reset	0x0							
Access Type	Read Only							
Bit	7	6	5	4	3	2	1	0
Field	DbgCnt[7:0]							
Reset	0x0							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
DbgCnt	15:0	Rx Lane Debug count type controlled by CfgRTestCtrl.RxCntTypeSel for lane # controlled by CfgRTestCtrl.RxCntLaneSel, loaded on setting CfgRTestCtrl. RxLoad to 1

CfgRLaneSet (0x480, 0x490, 0x4A0, 0x4B0, 0x4C0, 0x4D0)

Configure Rx Lane Settings

BIT	31	30	29	28	27	26	25	24
Field	LnSrc[4:0]					–	LkSel	LnEn
Reset	0x0					–	0x1	0x0
Access Type	Write, Read					–	Write, Read	Write, Read
Bit	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Field	–	–	–	–	–	–	–	–
Reset	–	–	–	–	–	–	–	–
Access Type	–	–	–	–	–	–	–	–
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**
Field	–	–	–	–	–	–	–	–
Reset	–	–	–	–	–	–	–	–
Access Type	–	–	–	–	–	–	–	–
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Field	–	–	LID[4:0]					LnRst
Reset	–	–	0x0					0x0
Access Type	–	–	Write, Read					Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
LnSrc	31:27	Physical Rx Lane number sourced for Logical Rx Lane at lane-to-sample mapping	
LkSel	25	ILA Lock Select Control	0: Lane is excluded from ILA process 1: Lane is included in ILA process based on FIFO write start, ILA is performed in subclass 0 by waiting for FIFO writes on all Lanes with this bit set
LnEn	24	Rx Lane Enable Control	0: Rx Lane is Disabled 1: Rx Lane is Enabled
LID	5:1	Lane ID for used for ILA sequence checking	
LnRst	0	Lane reset control	0: Rx Lane is not in reset 1: Rx Lane is in reset

CfgRLaneIntEn (0x484, 0x494, 0x4A4, 0x4B4, 0x4C4, 0x4D4)

Configure Rx Lane Interrupt Enables

BIT	31	30	29	28	27	26	25	24
Field	–	DContErr	–	PRBSerr	KContErr	FChkErr	LCfgErr	ILAerr
Reset	–	0x0	–	0x0	0x0	0x0	0x0	0x0
Access Type	–	Write, Read	–	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read
Bit	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Field	–	–	–	–	–	–	FIFOempty	FIFOfull
Reset	–	–	–	–	–	–	0x0	0x0
Access Type	–	–	–	–	–	–	Write, Read	Write, Read
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**
Field	–	–	–	–	–	–	–	–
Reset	–	–	–	–	–	–	–	–
Access Type	–	–	–	–	–	–	–	–
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Field	FrNSync	LnReAlign	FrReAlign	–	–	DISP	NIT	CGS
Reset	0x0	0x0	0x0	–	–	0x0	0x0	0x0
Access Type	Write, Read	Write, Read	Write, Read	–	–	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION
DContErr	30	Enable Interrupt on Rx Lane continuous D21.5 not-detect latched
PRBSerr	28	Enable Interrupt on Rx Lane SerDes interface PRBS error latched
KContErr	27	Enable Interrupt on Rx Lane continuous /K/ not-detect latched
FChkErr	26	Enable Interrupt on Rx Lane ILA sequence FCHK error latched
LCfgErr	25	Enable Interrupt on Rx Lane ILA sequence lane configuration error latched
ILAerr	24	Enable Interrupt on Rx Lane ILA sequence decode error latched
FIFOempty	17	Enable Interrupt on Rx Lane FIFO empty detected on FIFO depth smaller than RLinkRegs.CfgRFIFO.MinFD latched
FIFOfull	16	Enable Interrupt on Rx Lane FIFO full detected on FIFO depth greater than RLinkRegs.CfgRFIFO.MaxFD latched
FrNSync	7	Enable Interrupt on Frame synchronization state machine not in Sync real-time
LnReAlign	6	Enable Interrupt on Lane realignment occurred latched
FrReAlign	5	Enable Interrupt on Frame realignment occurred latched
DISP	2	Enable Interrupt on 8B10B Disparity error latched
NIT	1	Enable Interrupt on 8B10B NIT error latched
CGS	0	Enable Interrupt on Code Group Synchronization out of Sync latched

CfgRLaneMuteEn (0x488, 0x498, 0x4A8, 0x4B8, 0x4C8, 0x4D8)

Configure Rx Lane DAC Mute Enables

BIT	31	30	29	28	27	26	25	24
Field	–	DContErr	–	PRBSerr	KContErr	FChkErr	LCfgErr	ILAerr
Reset	–	0x0	–	0x0	0x0	0x0	0x0	0x0
Access Type	–	Write, Read	–	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read
Bit	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Field	–	–	–	–	–	–	FIFOempty	FIFOfull
Reset	–	–	–	–	–	–	0x0	0x0
Access Type	–	–	–	–	–	–	Write, Read	Write, Read
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**
Field	–	–	–	–	–	–	–	–
Reset	–	–	–	–	–	–	–	–
Access Type	–	–	–	–	–	–	–	–
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Field	FrNSync	LnReAlign	FrReAlign	–	–	DISP	NIT	CGS
Reset	0x0	0x0	0x0	–	–	0x0	0x0	0x0
Access Type	Write, Read	Write, Read	Write, Read	–	–	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION
DContErr	30	Enable Mute on Rx Lane continuous D21.5 not-detect latched
PRBSerr	28	Enable Mute on Rx Lane SerDes interface PRBS error latched
KContErr	27	Enable Mute on Rx Lane continuous /K/ not-detect latched
FChkErr	26	Enable Mute on Rx Lane ILA sequence FCHK error latched
LCfgErr	25	Enable Mute on Rx Lane ILA sequence lane configuration error latched
ILAerr	24	Enable Mute on Rx Lane ILA sequence decode error latched
FIFOempty	17	Enable Mute on Rx Lane FIFO empty detected on FIFO depth smaller than RLinkRegs.CfgRFIFO.MinFD latched
FIFOfull	16	Enable Mute on Rx Lane FIFO full detected on FIFO depth greater than RLinkRegs.CfgRFIFO.MaxFD latched
FrNSync	7	Enable Mute on Frame synchronization state machine not in Sync real-time
LnReAlign	6	Enable Mute on Lane realignment occurred latched
FrReAlign	5	Enable Mute on Frame realignment occurred latched
DISP	2	Enable Mute on 8B10B Disparity error latched
NIT	1	Enable Mute on 8B10B NIT error latched
CGS	0	Enable Mute on Code Group Synchronization out of Sync latched

StatRLane (0x48C, 0x49C, 0x4AC, 0x4BC, 0x4CC, 0x4DC)

Rx Lane Status Register

BIT	31	30	29	28	27	26	25	24
Field	–	DContErr	–	PRBSerr	KContErr	FChkErr	LCfgErr	ILAerr
Reset	–	0x0	–	0x0	0x0	0x0	0x0	0x0
Access Type	–	Write 0 to Clear, Read	–	Write 0 to Clear, Read	Write 0 to Clear, Read	Write 0 to Clear, Read	Write 0 to Clear, Read	Write 0 to Clear, Read
Bit	23	22	21	20	19	18	17	16
Field	–	–	–	–	–	–	FIFOempty	FIFOfull
Reset	–	–	–	–	–	–	0x0	0x0
Access Type	–	–	–	–	–	–	Write 0 to Clear, Read	Write 0 to Clear, Read
Bit	15	14	13	12	11	10	9	8
Field	–	–	FIFODepth[5:0]					
Reset	–	–	0x0					
Access Type	–	–	Read Only					
Bit	7	6	5	4	3	2	1	0
Field	FrNSync	LnReAlign	FrReAlign	–	–	DISP	NIT	CGS
Reset	0x0	0x0	0x0	–	–	0x0	0x0	0x0
Access Type	Read Only	Write 0 to Clear, Read	Write 0 to Clear, Read	–	–	Write 0 to Clear, Read	Write 0 to Clear, Read	Write 0 to Clear, Read

BITFIELD	BITS	DESCRIPTION
DContErr	30	Rx Lane continuous D21.5 not-detect latched
PRBSerr	28	Rx Lane SerDes interface PRBS error latched
KContErr	27	Rx Lane continuous /K/ not-detect latched
FChkErr	26	Rx Lane ILA sequence FCHK error latched
LCfgErr	25	Rx Lane ILA sequence lane configuration error latched
ILAerr	24	Rx Lane ILA sequence decode error latched
FIFOempty	17	Rx Lane FIFO empty detected on FIFO depth smaller than RLinkRegs.CfgRFIFO.MinFD latched
FIFOfull	16	Rx Lane FIFO full detected on FIFO depth greater than RLinkRegs.CfgRFIFO.MaxFD latched
FIFODepth	13:8	Rx Lane FIFO depth real-time updated when RLinkRegs.CfgRTestCtrl.SamLoad is set to 1
FrNSync	7	Frame synchronization state machine not in Sync real-time
LnReAlign	6	Lane realignment occurred latched
FrReAlign	5	Frame realignment occurred latched
DISP	2	8B10B Disparity error latched
NIT	1	8B10B NIT error latched
CGS	0	Code Group Synchronization out of Sync latched indicating that Lane configuration (excluding FCHK) described in section 8.3 of JESD204B-01 mismatches the local configuration

CfgSerDes (0x600)

SerDes common configuration for all lanes

BIT	31	30	29	28	27	26	25	24
Field	–	–	–	–	–	–	–	–
Reset	–	–	–	–	–	–	–	–
Access Type	–	–	–	–	–	–	–	–
Bit	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Field	–	–	–	–	–	–	RxRateSel[1:0]	
Reset	–	–	–	–	–	–	0x3	
Access Type	–	–	–	–	–	–	Write, Read	
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**
Field	–	–	–	–	–	–	–	–
Reset	–	–	–	–	–	–	–	–
Access Type	–	–	–	–	–	–	–	–
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Field	PhyWMode[1:0]		BCast[1:0]		–	PhyKill	–	Rst
Reset	0x0		0x0		–	0x0	–	0x1
Access Type	Write, Read		Write, Read		–	Write, Read	–	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
RxRateSel	17:16	Rx Rate select for CDR	0: Eighth rate 1: Quarter rate 2: Half rate 3: Full rate
PhyWMode	7:6	PHY 32-bit register interface write mode	0: Buffer upper-3 bytes and transfer all 4 bytes on write to byte0 1: Buffer lower-3 bytes and transfer all 4 bytes on write to byte3 2: Enable individual byte writes
BCast	5:4	PHY register broadcast write control	0: No Broadcast CPU writes to all PHYs 1: Broadcast CPU writes to all PHYs 2: Broadcast CPU writes to all PHYs enabled in RxLink 3: Reserved
PhyKill	2	SerDes PHY Kill control	0: SerDes PHY not in kill state 1: SerDes PHY in kill state
Rst	0	RLMS block Reset control	0: RLMS block not in reset state 1: RLMS block in reset state

CfgTrainAct (0x608)

Force activate training control

BIT	31	30	29	28	27	26	25	24
Field	–	–	–	–	–	–	–	–
Reset	–	–	–	–	–	–	–	–
Access Type	–	–	–	–	–	–	–	–
Bit	23	22	21	20	19	18	17	16
Field	–	–	–	–	–	–	–	–
Reset	–	–	–	–	–	–	–	–
Access Type	–	–	–	–	–	–	–	–
Bit	15	14	13	12	11	10	9	8
Field	–	–	–	–	–	–	–	–
Reset	–	–	–	–	–	–	–	–
Access Type	–	–	–	–	–	–	–	–
Bit	7	6	5	4	3	2	1	0
Field	–	–	Ln__5	Ln__4	Ln__3	Ln__2	Ln__1	Ln__0
Reset	–	–	0x0	0x0	0x0	0x0	0x0	0x0
Access Type	–	–	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
Ln__5	5	Force activate training for Lane N	0: Do not force training active 1: Force training active
Ln__4	4	Force activate training for Lane N	0: Do not force training active 1: Force training active
Ln__3	3	Force activate training for Lane N	0: Do not force training active 1: Force training active
Ln__2	2	Force activate training for Lane N	0: Do not force training active 1: Force training active
Ln__1	1	Force activate training for Lane N	0: Do not force training active 1: Force training active
Ln__0	0	Force activate training for Lane N	0: Do not force training active 1: Force training active

CfgTrainDeAct (0x60C)

Force activate training control

BIT	31	30	29	28	27	26	25	24
Field	–	–	–	–	–	–	–	–
Reset	–	–	–	–	–	–	–	–
Access Type	–	–	–	–	–	–	–	–
Bit	23	22	21	20	19	18	17	16
Field	–	–	–	–	–	–	–	–
Reset	–	–	–	–	–	–	–	–
Access Type	–	–	–	–	–	–	–	–
Bit	15	14	13	12	11	10	9	8
Field	–	–	–	–	–	–	–	–
Reset	–	–	–	–	–	–	–	–
Access Type	–	–	–	–	–	–	–	–
Bit	7	6	5	4	3	2	1	0
Field	–	–	Ln__5	Ln__4	Ln__3	Ln__2	Ln__1	Ln__0
Reset	–	–	0x1	0x1	0x1	0x1	0x1	0x1
Access Type	–	–	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
Ln__5	5	Force deactivate training for Lane N	0: Do not force training deactive 1: Force training deactive
Ln__4	4	Force deactivate training for Lane N	0: Do not force training deactive 1: Force training deactive
Ln__3	3	Force deactivate training for Lane N	0: Do not force training deactive 1: Force training deactive
Ln__2	2	Force deactivate training for Lane N	0: Do not force training deactive 1: Force training deactive
Ln__1	1	Force deactivate training for Lane N	0: Do not force training deactive 1: Force training deactive
Ln__0	0	Force deactivate training for Lane N	0: Do not force training deactive 1: Force training deactive

CfgIdleGate (0x610)

Gate data off to RxLink on SerDes SigDet control

BIT	31	30	29	28	27	26	25	24
Field	–	–	–	–	–	–	–	–
Reset	–	–	–	–	–	–	–	–
Access Type	–	–	–	–	–	–	–	–
Bit	23	22	21	20	19	18	17	16
Field	–	–	–	–	–	–	–	–
Reset	–	–	–	–	–	–	–	–
Access Type	–	–	–	–	–	–	–	–
Bit	15	14	13	12	11	10	9	8
Field	–	–	–	–	–	–	–	–
Reset	–	–	–	–	–	–	–	–
Access Type	–	–	–	–	–	–	–	–
Bit	7	6	5	4	3	2	1	0
Field	–	–	Ln__5	Ln__4	Ln__3	Ln__2	Ln__1	Ln__0
Reset	–	–	0x1	0x1	0x1	0x1	0x1	0x1
Access Type	–	–	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
Ln__5	5	Gate data off to RxLink on SerDes SigDet control for Lane N	0: Do no gate data off to RxLink on SerDes SigDet 1: Gate data off to RxLink when SerDes SigDet is high for lane N
Ln__4	4	Gate data off to RxLink on SerDes SigDet control for Lane N	0: Do no gate data off to RxLink on SerDes SigDet 1: Gate data off to RxLink when SerDes SigDet is high for lane N
Ln__3	3	Gate data off to RxLink on SerDes SigDet control for Lane N	0: Do no gate data off to RxLink on SerDes SigDet 1: Gate data off to RxLink when SerDes SigDet is high for lane N
Ln__2	2	Gate data off to RxLink on SerDes SigDet control for Lane N	0: Do no gate data off to RxLink on SerDes SigDet 1: Gate data off to RxLink when SerDes SigDet is high for lane N
Ln__1	1	Gate data off to RxLink on SerDes SigDet control for Lane N	0: Do no gate data off to RxLink on SerDes SigDet 1: Gate data off to RxLink when SerDes SigDet is high for lane N
Ln__0	0	Gate data off to RxLink on SerDes SigDet control for Lane N	0: Do no gate data off to RxLink on SerDes SigDet 1: Gate data off to RxLink when SerDes SigDet is high for lane N

CfgDoneGate (0x614)

Gate data off to RxLink on SerDes TrainDone control

BIT	31	30	29	28	27	26	25	24
Field	–	–	–	–	–	–	–	–
Reset	–	–	–	–	–	–	–	–
Access Type	–	–	–	–	–	–	–	–
Bit	23	22	21	20	19	18	17	16
Field	–	–	–	–	–	–	–	–
Reset	–	–	–	–	–	–	–	–
Access Type	–	–	–	–	–	–	–	–
Bit	15	14	13	12	11	10	9	8
Field	–	–	–	–	–	–	–	–
Reset	–	–	–	–	–	–	–	–
Access Type	–	–	–	–	–	–	–	–
Bit	7	6	5	4	3	2	1	0
Field	–	–	Ln__5	Ln__4	Ln__3	Ln__2	Ln__1	Ln__0
Reset	–	–	0x1	0x1	0x1	0x1	0x1	0x1
Access Type	–	–	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
Ln__5	5	Gate data off to RxLink on SerDes TrainDone control for Lane N	0: Do not gate data off to RxLink on SerDes TrainDone 1: Gate data off to RxLink when SerDes TrainDone is low for lane N
Ln__4	4	Gate data off to RxLink on SerDes TrainDone control for Lane N	0: Do not gate data off to RxLink on SerDes TrainDone 1: Gate data off to RxLink when SerDes TrainDone is low for lane N
Ln__3	3	Gate data off to RxLink on SerDes TrainDone control for Lane N	0: Do not gate data off to RxLink on SerDes TrainDone 1: Gate data off to RxLink when SerDes TrainDone is low for lane N
Ln__2	2	Gate data off to RxLink on SerDes TrainDone control for Lane N	0: Do not gate data off to RxLink on SerDes TrainDone 1: Gate data off to RxLink when SerDes TrainDone is low for lane N
Ln__1	1	Gate data off to RxLink on SerDes TrainDone control for Lane N	0: Do not gate data off to RxLink on SerDes TrainDone 1: Gate data off to RxLink when SerDes TrainDone is low for lane N
Ln__0	0	Gate data off to RxLink on SerDes TrainDone control for Lane N	0: Do not gate data off to RxLink on SerDes TrainDone 1: Gate data off to RxLink when SerDes TrainDone is low for lane N

CfgReserved (0x618)

CfgReserved for future use

BIT	31	30	29	28	27	26	25	24
Field	–	–	–	–	–	–	–	–
Reset	–	–	–	–	–	–	–	–
Access Type	–	–	–	–	–	–	–	–
Bit	23	22	21	20	19	18	17	16
Field	–	–	–	–	–	–	–	–
Reset	–	–	–	–	–	–	–	–
Access Type	–	–	–	–	–	–	–	–
Bit	15	14	13	12	11	10	9	8
Field	Rsvd[15:8]							
Reset	0x0							
Access Type	Write, Read							
Bit	7	6	5	4	3	2	1	0
Field	Rsvd[7:0]							
Reset	0x0							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
Rsvd	15:0	Reserved

CfgIntEnRLMS (0x61C)

Interrupt Enable register for RLMS block status

BIT	31	30	29	28	27	26	25	24
Field	–	–	–	–	–	–	–	–
Reset	–	–	–	–	–	–	–	–
Access Type	–	–	–	–	–	–	–	–
Bit	23	22	21	20	19	18	17	16
Field	–	–	–	–	–	–	–	–
Reset	–	–	–	–	–	–	–	–
Access Type	–	–	–	–	–	–	–	–
Bit	15	14	13	12	11	10	9	8
Field	–	–	–	–	–	–	–	–
Reset	–	–	–	–	–	–	–	–
Access Type	–	–	–	–	–	–	–	–
Bit	7	6	5	4	3	2	1	0
Field	–	–	Ln__5	Ln__4	Ln__3	Ln__2	Ln__1	Ln__0
Reset	–	–	0x0	0x0	0x0	0x0	0x0	0x0
Access Type	–	–	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION
Ln__5	5	Enable interrupt on RLMS status for Lane N
Ln__4	4	Enable interrupt on RLMS status for Lane N
Ln__3	3	Enable interrupt on RLMS status for Lane N
Ln__2	2	Enable interrupt on RLMS status for Lane N
Ln__1	1	Enable interrupt on RLMS status for Lane N
Ln__0	0	Enable interrupt on RLMS status for Lane N

CfgIntEnTrainDn (0x620)

Interrupt Enable register for Training Done status

BIT	31	30	29	28	27	26	25	24
Field	–	–	–	–	–	–	–	–
Reset	–	–	–	–	–	–	–	–
Access Type	–	–	–	–	–	–	–	–
Bit	23	22	21	20	19	18	17	16
Field	–	–	–	–	–	–	–	–
Reset	–	–	–	–	–	–	–	–
Access Type	–	–	–	–	–	–	–	–
Bit	15	14	13	12	11	10	9	8
Field	–	–	–	–	–	–	–	–
Reset	–	–	–	–	–	–	–	–
Access Type	–	–	–	–	–	–	–	–
Bit	7	6	5	4	3	2	1	0
Field	–	–	Ln__5	Ln__4	Ln__3	Ln__2	Ln__1	Ln__0
Reset	–	–	0x0	0x0	0x0	0x0	0x0	0x0
Access Type	–	–	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION
Ln__5	5	Enable interrupt on Training done for Lane N
Ln__4	4	Enable interrupt on Training done for Lane N
Ln__3	3	Enable interrupt on Training done for Lane N
Ln__2	2	Enable interrupt on Training done for Lane N
Ln__1	1	Enable interrupt on Training done for Lane N
Ln__0	0	Enable interrupt on Training done for Lane N

CfgIntEnSigDet (0x624)

Interrupt Enable register for Signal Detect status

BIT	31	30	29	28	27	26	25	24
Field	–	–	–	–	–	–	–	–
Reset	–	–	–	–	–	–	–	–
Access Type	–	–	–	–	–	–	–	–
Bit	23	22	21	20	19	18	17	16
Field	–	–	–	–	–	–	–	–
Reset	–	–	–	–	–	–	–	–
Access Type	–	–	–	–	–	–	–	–
Bit	15	14	13	12	11	10	9	8
Field	–	–	–	–	–	–	–	–
Reset	–	–	–	–	–	–	–	–
Access Type	–	–	–	–	–	–	–	–
Bit	7	6	5	4	3	2	1	0
Field	–	–	Ln__5	Ln__4	Ln__3	Ln__2	Ln__1	Ln__0
Reset	–	–	0x0	0x0	0x0	0x0	0x0	0x0
Access Type	–	–	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION
Ln__5	5	Enable interrupt on Signal Detect for Lane N
Ln__4	4	Enable interrupt on Signal Detect for Lane N
Ln__3	3	Enable interrupt on Signal Detect for Lane N
Ln__2	2	Enable interrupt on Signal Detect for Lane N
Ln__1	1	Enable interrupt on Signal Detect for Lane N
Ln__0	0	Enable interrupt on Signal Detect for Lane N

CfgMuteEnRLMS (0x628)

Mute Enable register for RLMS block status

BIT	31	30	29	28	27	26	25	24
Field	–	–	–	–	–	–	–	–
Reset	–	–	–	–	–	–	–	–
Access Type	–	–	–	–	–	–	–	–
Bit	23	22	21	20	19	18	17	16
Field	–	–	–	–	–	–	–	–
Reset	–	–	–	–	–	–	–	–
Access Type	–	–	–	–	–	–	–	–
Bit	15	14	13	12	11	10	9	8
Field	–	–	–	–	–	–	–	–
Reset	–	–	–	–	–	–	–	–
Access Type	–	–	–	–	–	–	–	–
Bit	7	6	5	4	3	2	1	0
Field	–	–	Ln__5	Ln__4	Ln__3	Ln__2	Ln__1	Ln__0
Reset	–	–	0x0	0x0	0x0	0x0	0x0	0x0
Access Type	–	–	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION
Ln__5	5	Enable DAC mute on RLMS status for Lane N
Ln__4	4	Enable DAC mute on RLMS status for Lane N
Ln__3	3	Enable DAC mute on RLMS status for Lane N
Ln__2	2	Enable DAC mute on RLMS status for Lane N
Ln__1	1	Enable DAC mute on RLMS status for Lane N
Ln__0	0	Enable DAC mute on RLMS status for Lane N

CfgMuteEnTrainDn (0x62C)

Mute Enable register for Training Done status

BIT	31	30	29	28	27	26	25	24
Field	–	–	–	–	–	–	–	–
Reset	–	–	–	–	–	–	–	–
Access Type	–	–	–	–	–	–	–	–
Bit	23	22	21	20	19	18	17	16
Field	–	–	–	–	–	–	–	–
Reset	–	–	–	–	–	–	–	–
Access Type	–	–	–	–	–	–	–	–
Bit	15	14	13	12	11	10	9	8
Field	–	–	–	–	–	–	–	–
Reset	–	–	–	–	–	–	–	–
Access Type	–	–	–	–	–	–	–	–
Bit	7	6	5	4	3	2	1	0
Field	–	–	Ln__5	Ln__4	Ln__3	Ln__2	Ln__1	Ln__0
Reset	–	–	0x0	0x0	0x0	0x0	0x0	0x0
Access Type	–	–	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION
Ln__5	5	Enable DAC mute on Training done for Lane N
Ln__4	4	Enable DAC mute on Training done for Lane N
Ln__3	3	Enable DAC mute on Training done for Lane N
Ln__2	2	Enable DAC mute on Training done for Lane N
Ln__1	1	Enable DAC mute on Training done for Lane N
Ln__0	0	Enable DAC mute on Training done for Lane N

CfgMuteEnSigDet (0x630)

Mute Enable register for Signal Detect status

BIT	31	30	29	28	27	26	25	24
Field	–	–	–	–	–	–	–	–
Reset	–	–	–	–	–	–	–	–
Access Type	–	–	–	–	–	–	–	–
Bit	23	22	21	20	19	18	17	16
Field	–	–	–	–	–	–	–	–
Reset	–	–	–	–	–	–	–	–
Access Type	–	–	–	–	–	–	–	–
Bit	15	14	13	12	11	10	9	8
Field	–	–	–	–	–	–	–	–
Reset	–	–	–	–	–	–	–	–
Access Type	–	–	–	–	–	–	–	–
Bit	7	6	5	4	3	2	1	0
Field	–	–	Ln__5	Ln__4	Ln__3	Ln__2	Ln__1	Ln__0
Reset	–	–	0x0	0x0	0x0	0x0	0x0	0x0
Access Type	–	–	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION
Ln__5	5	Enable DAC mute on Signal Detect for Lane N
Ln__4	4	Enable DAC mute on Signal Detect for Lane N
Ln__3	3	Enable DAC mute on Signal Detect for Lane N
Ln__2	2	Enable DAC mute on Signal Detect for Lane N
Ln__1	1	Enable DAC mute on Signal Detect for Lane N
Ln__0	0	Enable DAC mute on Signal Detect for Lane N

StatRLMS (0x634)

RLMS status register

BIT	31	30	29	28	27	26	25	24
Field	–	–	–	–	–	–	–	–
Reset	–	–	–	–	–	–	–	–
Access Type	–	–	–	–	–	–	–	–
Bit	23	22	21	20	19	18	17	16
Field	–	–	–	–	–	–	–	–
Reset	–	–	–	–	–	–	–	–
Access Type	–	–	–	–	–	–	–	–
Bit	15	14	13	12	11	10	9	8
Field	–	–	–	–	–	–	–	–
Reset	–	–	–	–	–	–	–	–
Access Type	–	–	–	–	–	–	–	–
Bit	7	6	5	4	3	2	1	0
Field	–	–	Ln__5	Ln__4	Ln__3	Ln__2	Ln__1	Ln__0
Reset	–	–	0x0	0x0	0x0	0x0	0x0	0x0
Access Type	–	–	Read Only	Read Only	Read Only	Read Only	Read Only	Read Only

BITFIELD	BITS	DESCRIPTION
Ln__5	5	RLMS combined status real-time for Lane N
Ln__4	4	RLMS combined status real-time for Lane N
Ln__3	3	RLMS combined status real-time for Lane N
Ln__2	2	RLMS combined status real-time for Lane N
Ln__1	1	RLMS combined status real-time for Lane N
Ln__0	0	RLMS combined status real-time for Lane N

StatTrainDn (0x638)

Training done status register latched

BIT	31	30	29	28	27	26	25	24
Field	–	–	–	–	–	–	–	–
Reset	–	–	–	–	–	–	–	–
Access Type	–	–	–	–	–	–	–	–
Bit	23	22	21	20	19	18	17	16
Field	–	–	–	–	–	–	–	–
Reset	–	–	–	–	–	–	–	–
Access Type	–	–	–	–	–	–	–	–
Bit	15	14	13	12	11	10	9	8
Field	–	–	–	–	–	–	–	–
Reset	–	–	–	–	–	–	–	–
Access Type	–	–	–	–	–	–	–	–
Bit	7	6	5	4	3	2	1	0
Field	–	–	Ln__5	Ln__4	Ln__3	Ln__2	Ln__1	Ln__0
Reset	–	–	0x0	0x0	0x0	0x0	0x0	0x0
Access Type	–	–	Read Only	Read Only	Read Only	Read Only	Read Only	Read Only

BITFIELD	BITS	DESCRIPTION
Ln__5	5	Training done latched status for Lane N
Ln__4	4	Training done latched status for Lane N
Ln__3	3	Training done latched status for Lane N
Ln__2	2	Training done latched status for Lane N
Ln__1	1	Training done latched status for Lane N
Ln__0	0	Training done latched status for Lane N

StatSigDet (0x63C)

SerDes Signal Detect real-time status register

BIT	31	30	29	28	27	26	25	24
Field	–	–	–	–	–	–	–	–
Reset	–	–	–	–	–	–	–	–
Access Type	–	–	–	–	–	–	–	–
Bit	23	22	21	20	19	18	17	16
Field	–	–	–	–	–	–	–	–
Reset	–	–	–	–	–	–	–	–
Access Type	–	–	–	–	–	–	–	–
Bit	15	14	13	12	11	10	9	8
Field	–	–	–	–	–	–	–	–
Reset	–	–	–	–	–	–	–	–
Access Type	–	–	–	–	–	–	–	–
Bit	7	6	5	4	3	2	1	0
Field	–	–	Ln__5	Ln__4	Ln__3	Ln__2	Ln__1	Ln__0
Reset	–	–	0x0	0x0	0x0	0x0	0x0	0x0
Access Type	–	–	Read Only	Read Only	Read Only	Read Only	Read Only	Read Only

BITFIELD	BITS	DESCRIPTION
Ln__5	5	High indicates phy RX receivers are below the LOS threshold on Lane N
Ln__4	4	High indicates phy RX receivers are below the LOS threshold on Lane N
Ln__3	3	High indicates phy RX receivers are below the LOS threshold on Lane N
Ln__2	2	High indicates phy RX receivers are below the LOS threshold on Lane N
Ln__1	1	High indicates phy RX receivers are below the LOS threshold on Lane N
Ln__0	0	High indicates phy RX receivers are below the LOS threshold on Lane N

CfgCMU1 (0x644)

Configure CMU word 1

BIT	31	30	29	28	27	26	25	24
Field	Rsvd1	–	–	–	–	cd_tune1p0[2:0]		
Reset	0x0	–	–	–	–	0x0		
Access Type	Write, Read	–	–	–	–	Write, Read		
Bit	23	22	21	20	19	18	17	16
Field	Cref_divsel1p0[1:0]		–	–	Rsvd0[13:10]			
Reset	0x0		–	–	0x0			
Access Type	Write, Read		–	–	Write, Read			
Bit	15	14	13	12	11	10	9	8
Field	Rsvd0[9:2]							
Reset	0x0							
Access Type	Write, Read							
Bit	7	6	5	4	3	2	1	0
Field	Rsvd0[1:0]		FBDIV[1:0]		VCOSEL[1:0]		–	–
Reset	0x0		0x0		0x0		–	–
Access Type	Write, Read		Write, Read		Write, Read		–	–

BITFIELD	BITS	DESCRIPTION	DECODE
Rsvd1	31	Reserved 1	
cd_tune1p0	26:24	Clocktree tunning for center freq	0: 10G 4: 7G 7: 6G
Cref_divsel1p0	23:22	Refclk path divider selection	0: CMU refclk divide by 1 1: CMU refclk divide by 2 2: CMU refclk divide by 4 3: CMU refclk divide by 8
Rsvd0	19:6	Reserved 0	
FBDIV	5:4	Feedback divider control	0: Divide by 40 1: Divide by 80 3: Divide by 20
VCOSEL	3:2	VCO select	0: 10G VCO 1: 10G VCO 2: 7G VCO 3: 6G VCO

EQU_CTRL3 (0x80C, 0x90C, 0xA0C, 0xB0C, 0xC0C, 0xD0C)

Equalizer Control 3

BIT	31	30	29	28	27	26	25	24
Field	Reserved[1:0]		D1_coeff[5:0]					
Reset	0x0		0x4					
Access Type	Write, Read		Write, Read					
Bit	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Field	Reserved	D2_coeff[6:0]						
Reset	0x0	0x0						
Access Type	Write, Read	Write, Read						
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**
Field	Reserved	D3_coeff[6:0]						
Reset	0x0	0x0						
Access Type	Write, Read	Write, Read						
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Field	Reserved	D4_coeff[6:0]						
Reset	0x0	0x0						
Access Type	Write, Read	Write, Read						

BITFIELD	BITS	DESCRIPTION
Reserved	31:30	Reserved for factory use
D1_coeff	29:24	DFE coefficient D1, binary-encoded magnitude, negativegain only. Drives a 6-bit magnitude DAC.Example values: 6'h00 = 0 amplitude 6'h3F = maximum negative amplitude -0.5
Reserved	23	Reserved for factory use
D2_coeff	22:16	DFE coefficient D2 sign/binary-encoded magnitude.Drives a 7-bit DAC with the highest bitrepresenting the sign.Example values: 7'h3F = maximum positive amplitude = 0.25 7'h01 = smallest positive amplitude = 0.25/63 7'h00 = 0 amplitude 7'h41 = smallest negative amplitude = -0.25/63 7'h7F = maximum negative amplitude = -0.25
Reserved	15	Reserved for factory use
D3_coeff	14:8	DFE coefficient D3 sign/binary-encoded magnitude.Drives a 7-bit DAC with the highest bitrepresenting the sign. See D2_coeff above for examples.
Reserved	7	Reserved for factory use
D4_coeff	6:0	DFE coefficient D4 sign/binary-encoded magnitude.Drives a 7-bit DAC with the highest bitrepresenting the sign. See D2_coeff above for examples.

EQU_CTRL4 (0x810, 0x910, 0xA10, 0xB10, 0xC10, 0xD10)

Equalizer Control 4

BIT	31	30	29	28	27	26	25	24
Field	Reserved	Reserved[6:0]						
Reset	0x0	0x0						
Access Type	Write, Read	Write, Read						
Bit	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Field	Reserved[9:2]							
Reset	0x0							
Access Type	Write, Read							
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**
Field	Reserved[1:0]		Reserved[5:0]					
Reset	0x0		0x7					
Access Type	Write, Read		Write, Read					
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Field	AGC_coeff[7:0]							
Reset	0x80							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
Reserved	31	Reserved for factory use
Reserved	30:24	Reserved for factory use, should be set to 0x45
Reserved	23:14	Reserved for factory use
Reserved	13:8	Reserved for factory use, should be set to 0x10
AGC_coeff	7:0	VGA gain, binary encoded.00h = +10 db (NOTE THIS INVERSION IS INTENTIONAL!) FFh = -10 db

EQU_CTRL7 (0x81C, 0x91C, 0xA1C, 0xB1C, 0xC1C, 0xD1C)

Equalizer Control 7

BIT	31	30	29	28	27	26	25	24
Field	AGC_init_D1[7:0]							
Reset	0x81							
Access Type	Write, Read							
Bit	23	22	21	20	19	18	17	16
Field	Reserved[7:0]							
Reset	0xFF							
Access Type	Write, Read							
Bit	15	14	13	12	11	10	9	8
Field	Reserved[1:0]		Reserved[5:0]					
Reset	0x0		0x2					
Access Type	Write, Read		Write, Read					
Bit	7	6	5	4	3	2	1	0
Field	Reserved[7:0]							
Reset	0x0							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
AGC_init_D1	31:24	Full-Rate AGC initialization value. This value is the value loaded on an LOS event.
Reserved	23:16	Reserved for factory use, should be set o 0xFF
Reserved	15:14	Reserved for factory use
Reserved	13:8	Reserved for factory use, should be set to 0x08
Reserved	7:0	Reserved for factory use, should be set to 0x00

EQU_CTRLA (0x828, 0x928, 0xA28, 0xB28, 0xC28, 0xD28)

Equalizer Control A

BIT	31	30	29	28	27	26	25	24
Field	Reserved[1:0]		D1_init[5:0]					
Reset	0x0		0x0					
Access Type	Write, Read		Write, Read					
Bit	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Field	Reserved	D2_init[6:0]						
Reset	0x0	0x0						
Access Type	Write, Read	Write, Read						
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**
Field	Reserved	D3_init[6:0]						
Reset	0x0	0x0						
Access Type	Write, Read	Write, Read						
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Field	Reserved	D4_init[6:0]						
Reset	0x0	0x0						
Access Type	Write, Read	Write, Read						

BITFIELD	BITS	DESCRIPTION
Reserved	31:30	Reserved for factory use, should be set to 0x1
D1_init	29:24	Full-Rate D1 initialization value. See D1_coeff for format (register 0x0C). This value is the value loaded on an LOS event.
Reserved	23	Reserved for factory use
D2_init	22:16	Full-Rate D2 initialization value. See D2_coeff for format (register 0x0C). This value is the value loaded on an LOS event.
Reserved	15	Reserved for factory use
D3_init	14:8	Full-Rate D3 initialization value. See D2_coeff for format (register 0x0C). This value is the value loaded on an LOS event.
Reserved	7	Reserved for factory use
D4_init	6:0	Full-Rate D4 initialization value. See D2_coeff for format (register 0x0C). This value is the value loaded on an LOS event.

EQU_CTRLB (0x82C, 0x92C, 0xA2C, 0xB2C, 0xC2C, 0xD2C)

Equalizer Control B

BIT	31	30	29	28	27	26	25	24
Field	Reserved[1:0]		Reserved[1:0]		capsel[1:0]		Mode6Gphb	Reserved
Reset	0x0		0x0		0x0		0x0	0x0
Access Type	Write, Read		Write, Read		Write, Read		Write, Read	Write, Read
Bit	23	22	21	20	19	18	17	16
Field	Reserved[1:0]		Reserved[5:0]					
Reset	0x0		0x0					
Access Type	Write, Read		Write, Read					
Bit	15	14	13	12	11	10	9	8
Field	Reserved[7:0]							
Reset	0x0							
Access Type	Write, Read							
Bit	7	6	5	4	3	2	1	0
Field	Reserved[7:0]							
Reset	0x0							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
Reserved	31:30	Reserved for factory use
Reserved	29:28	Reserved for factory use
capsel	27:26	Error slicer phase interpolator capacitor setting0X = use for 2.457G (9.83G/4), 3.684G (7.3728G/2) and 3.072 (6.144G/2)10 = use for 4.915G (9.83G/2), 6.144G, and 7.372G11 = use for 9.83G
Mode6Gphb	25	PHY clock phase interpolator coarse tuning for 6GHz0 = use for 6GHz and 7GHz CMU1 = use for 9.8GHz CMU
Reserved	24	Reserved for factory use
Reserved	23:22	Reserved for factory use
Reserved	21:16	Reserved for factory use, should be set to 0x1F
Reserved	15:8	Reserved for factory use
Reserved	7:0	Reserved for factory use

EYE_MON2 (0x83C, 0x93C, 0xA3C, 0xB3C, 0xC3C, 0xD3C)

Eye Monitor 2

BIT	31	30	29	28	27	26	25	24
Field	D1ErrChPhPri[7:0]							
Reset	0xBB							
Access Type	Write, Read							
Bit	23	22	21	20	19	18	17	16
Field	D1ErrChPhSec[7:0]							
Reset	0x40							
Access Type	Write, Read							
Bit	15	14	13	12	11	10	9	8
Field	Reserved[7:0]							
Reset	0xCE							
Access Type	Write, Read							
Bit	7	6	5	4	3	2	1	0
Field	Reserved	Reserved[6:0]						
Reset	0x1	0x3						
Access Type	Write, Read	Write, Read						

BITFIELD	BITS	DESCRIPTION
D1ErrChPhPri	31:24	Primary error (even) channel phase command
D1ErrChPhSec	23:16	Secondary error (odd) channel phase command. Thisplaces the error channel one UI behind the primarysampling phase.
Reserved	15:8	Reserved for factory use, should be set to 0xAF
Reserved	7	Reserved for factory use
Reserved	6:0	Reserved for factory use

CLK_CTRL1 (0x864, 0x964, 0xA64, 0xB64, 0xC64, 0xD64)

Clock Control 1

BIT	31	30	29	28	27	26	25	24
Field	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
Reset	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0
Access Type	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read
Bit	23	22	21	20	19	18	17	16
Field	Reserved	Reserved	Reserved	Reserved	Reserved[3:0]			
Reset	0x0	0x0	0x0	0x0	0x0			
Access Type	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read			
Bit	15	14	13	12	11	10	9	8
Field	Reserved[3:0]				Reserved	cd_tune[2:0]		
Reset	0x0				0x1	0x7		
Access Type	Write, Read				Write, Read	Write, Read		
Bit	7	6	5	4	3	2	1	0
Field	Reserved[3:0]				Reserved	Reserved	Reserved[1:0]	
Reset	0x0				0x0	0x0	0x0	
Access Type	Write, Read				Write, Read	Write, Read	Write, Read	

BITFIELD	BITS	DESCRIPTION
Reserved	31	Reserved for factory use
Reserved	30	Reserved for factory use
Reserved	29	Reserved for factory use
Reserved	28	Reserved for factory use
Reserved	27	Reserved for factory use
Reserved	26	Reserved for factory use
Reserved	25	Reserved for factory use
Reserved	24	Reserved for factory use
Reserved	23	Reserved for factory use
Reserved	22	Reserved for factory use, should be set to 1
Reserved	21	Reserved for factory use
Reserved	20	Reserved for factory use
Reserved	19:16	Reserved for factory use
Reserved	15:12	Reserved for factory use
Reserved	11	Reserved for factory use, should be set to 1
cd_tune	10:8	Clock driver frequency tuning111 = use when 6.14GHz CMU active100 = use when 7.37GHz CMU active000 = use when 9.83GHz CMU active
Reserved	7:4	Reserved for factory use, should be set to 0xC
Reserved	3	Reserved for factory use
Reserved	2	Reserved for factory use
Reserved	1:0	Reserved for factory use

EQU_CTRLD (0x880, 0x980, 0xA80, 0xB80, 0xC80, 0xD80)

Equalizer Control D

BIT	31	30	29	28	27	26	25	24
Field	Reserved[1:0]		DFE2_initD3[5:0]					
Reset	0x0		0x0					
Access Type	Write, Read		Write, Read					
Bit	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Field	Reserved	DFE2_initD2[6:0]						
Reset	0x0	0x0						
Access Type	Write, Read	Write, Read						
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**
Field	Reserved	DFE1_initD3[6:0]						
Reset	0x0	0x0						
Access Type	Write, Read	Write, Read						
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Field	Reserved	DFE1_initD2[6:0]						
Reset	0x0	0x0						
Access Type	Write, Read	Write, Read						

BITFIELD	BITS	DESCRIPTION
Reserved	31:30	Reserved for factory use, should be set to 0x1
DFE2_initD3	29:24	Quarter-rate DFE2 initialization value.
Reserved	23	Reserved for factory use
DFE2_initD2	22:16	Half-rate DFE2 initialization value.
Reserved	15	
DFE1_initD3	14:8	Quarter-rate DFE1 initialization value.
Reserved	7	Reserved for factory use
DFE1_initD2	6:0	Half-rate DFE1 initialization value.

EQU_CTRLE (0x884, 0x984, 0xA84, 0xB84, 0xC84, 0xD84)

Equalizer Control E

BIT	31	30	29	28	27	26	25	24
Field	Reserved	DFE4Init_D3[6:0]						
Reset	0x0	0x0						
Access Type	Write, Read	Write, Read						
Bit	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Field	Reserved	DFE4Init_D2[6:0]						
Reset	0x0	0x0						
Access Type	Write, Read	Write, Read						
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**
Field	Reserved	DFE3Init_D3[6:0]						
Reset	0x0	0x0						
Access Type	Write, Read	Write, Read						
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Field	Reserved	DFE3Init_D2[6:0]						
Reset	0x0	0x0						
Access Type	Write, Read	Write, Read						

BITFIELD	BITS	DESCRIPTION
Reserved	31	Reserved for factory use
DFE4Init_D3	30:24	Quarter-rate DFE4 coefficient initial value
Reserved	23	Reserved for factory use
DFE4Init_D2	22:16	Half-rate DFE4 coefficient initial value
Reserved	15	Reserved for factory use
DFE3Init_D3	14:8	Quarter-rate DFE3 coefficient initial value
Reserved	7	Reserved for factory use
DFE3Init_D2	6:0	Half-rate DFE3 coefficient initial value

EQU_CTRLG (0x88C, 0x98C, 0xA8C, 0xB8C, 0xC8C, 0xD8C)

Equalizer Control G

BIT	31	30	29	28	27	26	25	24
Field	Reserved[7:0]							
Reset	0x0							
Access Type	Write, Read							
Bit	23	22	21	20	19	18	17	16
Field	Reserved[7:0]							
Reset	0x0							
Access Type	Write, Read							
Bit	15	14	13	12	11	10	9	8
Field	AGCInit_D3[7:0]							
Reset	0x83							
Access Type	Write, Read							
Bit	7	6	5	4	3	2	1	0
Field	AGCInit_D2[7:0]							
Reset	0x82							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
Reserved	31:24	Reserved for factory use
Reserved	23:16	Reserved for factory use
AGCInit_D3	15:8	Quarter-rate AGC initialization value.
AGCInit_D2	7:0	Half-rate AGC initialization value.

Applications Information

JESD204B LINK and DSP Clocking

Subclass-0 with Device Clock

When there is a device clock present on the CLKP/CLKN pins, the Rx LINK sample clock is generated from the input clock. The DSP input FIFO removes the phase difference between the Rx LINK sample clock and DSP sample clock. This clock source mode is set by programming the RLinkRegs.CfgRLinkCtrl.rclk register to 0. The DSP sample clock will be stable when the DAC clock is stable, either through or bypassing the DAC PLL, while the interpolation mode is programmed within the DSP.CfgDSP.R[4:0] register. The Rx LINK sample clock will be stable once the device clock (DCLK) divide mode has been set with the RLinkRegs.CfgRLinkSet.Ddiv register.

Once these clocks for the DSP Input FIFO are stable, they need to be reset so the FIFOs can be centered. The Rx LINK Lane FIFOs are controlled by the Subclass-0 behavior providing minimal latency through the FIFO. The FIFO latency can be increased by programming the RLinkRegs.CfgRLinkMFrame.ILADly register with incremental frame clock periods. The following steps are required to configure the device for stable operation:

- If the DAC PLL is used, program the DAC PLL registers (DSP.CfgPLL)
- Program the Rx LINK device clock divide factor (RLinkRegs.CfgRLinkSet.Ddiv)
- Set the interpolation mode and then reset the input FIFO (DSP.CfgDSP.R[3:0], DSP.CfgDSP.RstFIFO)
- Remove the DSP input FIFO reset (DSP.CfgDSP.RstFIFO)

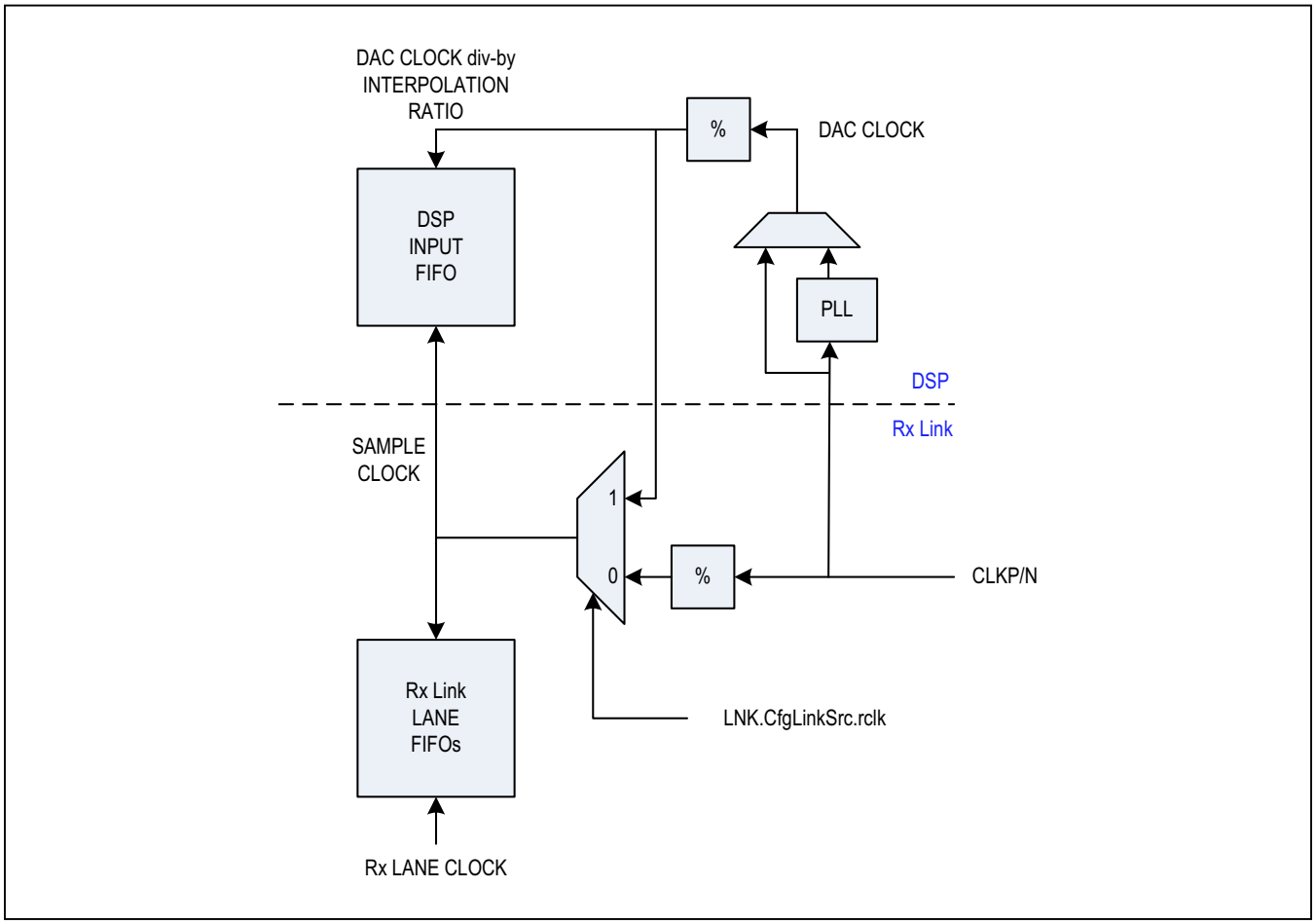


Figure 32. Rx LINK and DSP Clocking

Subclass-0 without Device Clock

When no device clock is present on the CLKP/CLKN pins, the Rx LINK sample clock is generated from the DSP sample clock. This source mode is set by programming the RLinkRegs.CfgRLinkCtrl.rclk register to 1. The DSP sample clock will be stable when DAC clock is stable, either through or bypassing the DAC PLL, while the interpolation mode is programmed within the DSP. CfgDSP.R[4:0] register. Once this clock for the DSP Input FIFO (same write and read clock) is stable, it needs to be centered by toggling the DSP reset DSP.CfgDSP.RstDSP. The Rx LINK lane FIFOs are controlled by the Subclass-0 behavior providing minimal latency through the FIFO. The FIFO latency can be increased by programming the RLinkRegs.CfgRLinkMFrame.ILADly register with with incremental frame clock periods. The following steps are required to configure the device for stable operation:

- If the DAC PLL is used, program the DAC PLL registers (DSP.CfgPLL)
- Set the interpolation mode (DSP.CfgDSP.R[3:0])
- Set the Rx LINK clock mode (RLinkRegs. CfgRLinkCtrl.rclk = 1)

Typical Configuration

The MAX5857 includes setting up the clocking as described in the following sections, as well as setting all other configurations before or after that. Configuration registers other than the clocking includes the DSP, JESD204B CMU, SerDes and LNK registers.

Enabling the DAC Output from Power-Up

The following is the overall flowchart from power-up to DAC output enable. Some of the intermediate steps are mode-specific and are described below.

Power Up: Ramp up power for all supplies, this does not require any particular order.

Chip Reset: Assert chip reset (RESETB) for 1µs. After reset is release, either monitor the INTB pin for a high-to-low transition or poll the DSP.STATUS.TRDY bit for a set (logic-high) state. These indicate that trimming is complete and the device is ready for configuration.

Clock Setup: Clock setup includes configuring the clock sources for internal blocks such as the DAC, the DSP, and the JESD204B functions. The JESD configuration must must also include the subclass mode since that configuration determines how the FIFOs are initialized. The Clock Setup sequence must include the following:

- DAC PLL usage
- Device Clock availability for JESD204B function
- DSP interpolation rate

Depending on the source used for generating the sample clock, Figure 34 shows the JESD204B setups sequences required for Subclass-0 operation.

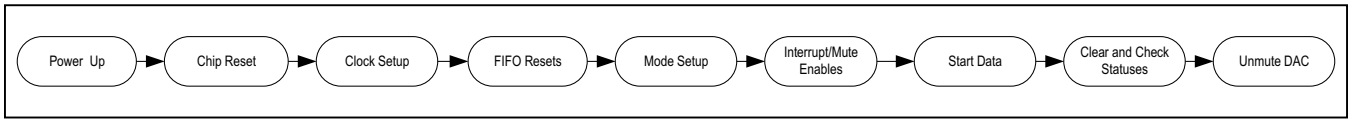


Figure 33. DAC Power-Up Sequence

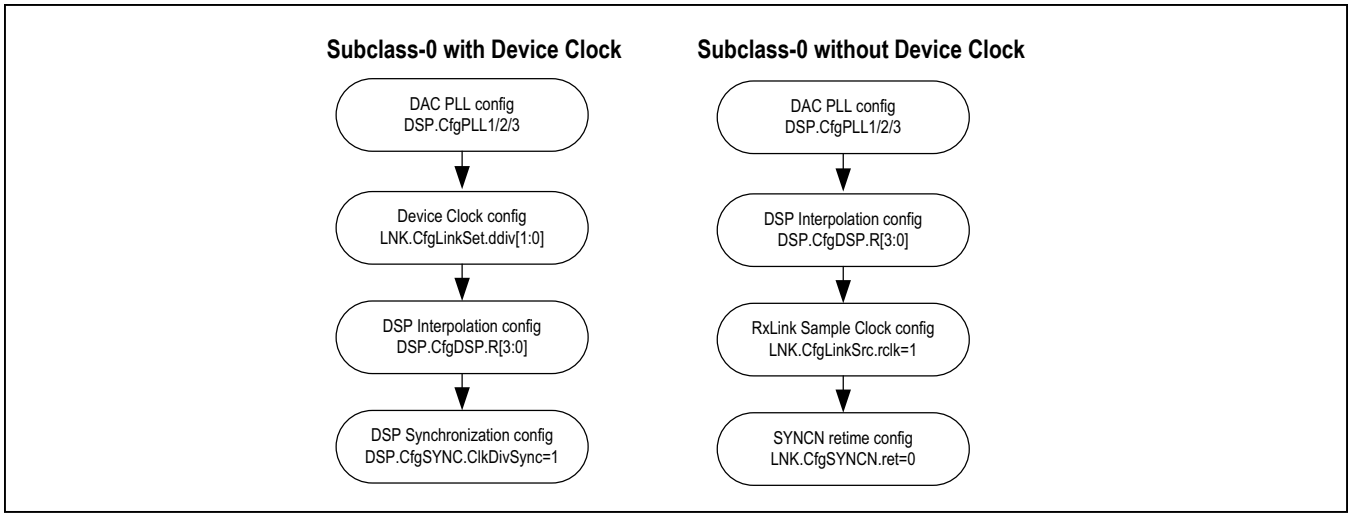


Figure 34. DAC Configuration Sequence

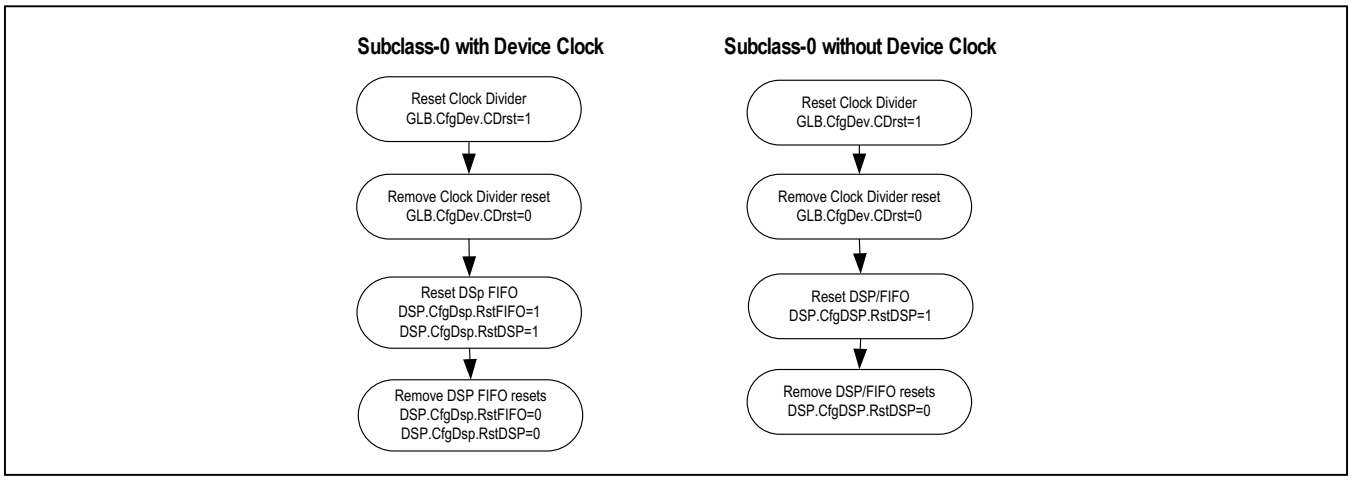


Figure 35. DAC Reset Sequence

FIFO Resets: After the clock modes are configured and after a sufficient wait time has passed to allow the DAC PLL to lock, the DSP clock divider needs to be reset. Next the Rx LINK and DSP FIFOs need to be centered through the configuration process of Subclass-0 mode. Depending on the sample clock source, the setups shown in Figure 34 are used for Subclass-0.

Mode Setup: Setup device modes other than DAC PLL, clocking, synchronization and resets.

Interrupt/Mute Enables: Enable internal DAC mute and interrupt-enable bits in the JESD204B RxLink and DSP registers.

Start Data: Start the JESD204B LINK carrying the digital data streams.

Clear and Check Statuses: Clear all the latched status bits which were previously enabled for internal DAC mute and interrupt.

Unmute DAC: Clear the DAC mute register bit (DSP. CfgChipOM.Mute) to enable the DAC output.

Applications Guidelines

Power Sequence

The MAX5857 does not require a specific power sequence. However, it is recommended that all the supplies are powered up simultaneously.

Power Supply AVCLK

Power for AVCLK is the most sensitive supply due to the sensitivity of the internal clock circuitry. To achieve the specified DAC performance, *AVCLK should not be shared with other 1.0V supplies*. In particular *the AVCLK supply must not be shared with digital VDD 1.0V supply.*

Power-On RESETB and SPI Configuration

During the initial power-on, the RESETB pin should be held low. The RESETB pin has an internal 32kΩ pulldown resistor and it should be pulled high only after all power supplies have stabilized at their nominal levels.

An alternative method for power-on-reset is to cycle the RESETB pin (transition high-to-low-to-high) after the power supplies are fully stabilized at their nominal levels.

There is a delay time required after the RESETB is set high, before SPI configuration can be initiated. The delay time allows the device to finish its initialization process. The delay is directly related to the CLKP/CLKN frequency, requiring about 370k clock cycles or about 250µs when using a device clock frequency of 1.47GHz.

A series of specific SPI writes must be performed each time the device is powered-up. These writes perform initialization of specific internal blocks and ensure consistent performance after every power cycle. These writes are generated by the configuration script described in the *Configuration Script Tool* section and should include the following command sequence:

Write 0x0206, 0x18
Write 0x0211, 0x8C
Write 0x0213, 0x40
Wait 100µs
Write 0x0213, 0x00
Write 0x0206, 0x0
Write 0x0211, 0x0
Wait 100µs

Delay Time $T_{D\text{-}DivRst}$ Estimation

Adding proper delay time before resetting the internal divider is important to ensure the divider starts with a stable clock. This allows the DAC PLL (or external CLKP/CLKN) to fully lock and settle. The minimum delay time is estimated as:

$$t_{D\ -\ DivRst} \approx \frac{220}{f_{PFD}} \quad (9)$$

Where f_{PFD} is the input frequency of the DAC PLL Phase Frequency Detector, when in PLL-on mode.

For example: when the CLKP/CLKN frequency is at 982.68MHz and the reference divider RVAL is set to 1/4, f_{PFD} = 982.68/4 = 245.67MHz. The $t_{D\text{-}DivRst}$ is estimated to be 0.9µs.

For the Configuration Script Tool output, a default delay of 20ms is used.

Pin DACREF Consideration

The 960Ω resistor from FSADJ (B2) should connect directly to DACREF (B1). This should be placed on the same side of the printed circuit board (PCB) as the MAX5857 package itself, and as close as possible to those pins. The 1µF capacitors which are connected to REFIO (A1) and CSBP (A2) should be connected to DACREF, **not GND**. These capacitors should also be placed on the same layer of the PCB as the DAC, avoiding vias on all these traces if possible. DACREF is internally connected to AGND. **DO NOT CONNECT DACREF TO EXTERNAL GROUND**.

DAC PLL Consideration

The PLL_COMP (A12) and VCOBYP (B11) connections form the loop filter for the PLL (see Figure 30). Place these external components on the PCB layer opposite the CLK and OUTPUT circuits (bottom versus top of the board) to prevent crosstalk coupling. The recommended filter between PLL_COMP (A12) and VCOBYP (B11) is a 2.7kΩ resistor in series with a 430pF capacitor. The C1 capacitor reduces noise from GND (A11) to VCOBYP (B11). Place C1 directly under the balls/vias of the package to make the physical loop (trace length) as small as possible. The exact values of C1 and C2 will vary depending on PCB layout and they may not be required for optimal performance.

Pin SDO Consideration

In 4-wire SPI interface mode, SDO is used as a serial data output. When connecting multiple SDOs together using CSB to access the MAX5857, it is recommended to have a 10kΩ pullup resistor on the input of FPGA or ASIC to prevent floating. When SDO is not selected, it remains high-impedance.

Clock Requirement

The MAX5857 can be operated with the internal DAC PLL on or off (bypassed). Care should always be taken to design the system using a low phase noise, low jitter clock source.

When DAC PLL is bypassed, phase noise and jitter from the clock source will directly affect the performance of the RF DAC. Phase noise introduces sample timing uncertainty in the converter which show up as noise “skirts” concentrated very close to the frequency of the output signal. Alternatively, wide-band jitter will cause an elevated noise floor in the DAC output with a flat power spectral density (white noise). The affects of wide-band jitter can be determined using the following equations:

$$SNR = 20 \cdot \log\left(\frac{\sqrt{12}}{2\pi\sigma_t\sqrt{f_{BW}^2 + 12f_C^2}}\right) \quad (10)$$

Where SNR [dB] is the Signal to Noise Ratio, σ_t [s] is the RMS jitter, f_{BW} [Hz] is the stationary signal bandwidth, and f_C [Hz] is the DAC output frequency

$$ND = P_{FS} + P_S + 20 \cdot \log\left(\mathrm{sinc}\left(\frac{\pi f_C}{f_S}\right)\right) - SNR - 10 \cdot \log\left(\frac{f_S}{2}\right) \quad (11)$$

Where ND [dBm/Hz] is the Noise Density in the 1st Nyquist zone, P_{FS} [dBm] is the DAC full scale output power (measured with a CW signal at $f_C << f_S/2$), P_S [dBFS] is the power of the digital input signal to the DAC referred to the full scale CW signal, and f_S [Hz] is the DAC sampling clock frequency

When DAC PLL is on, the DAC PLL bandwidth is set to around 1MHz (based on the loop filter components). This means that any phase noise or jitter of the reference clock at frequency offsets higher than 1MHz should be filtered out by the PLL loop thus any impact on the DAC performance will be minimized.

However, within the sub-1MHz band, the reference clock phase noise will dominate the PLL performance just as it would with full-band effects in PLL-bypass mode. In either case, the reference clock phase noise will be translated to the DAC output phase noise according to the formula:

$$PN_{OUT} = PN_{REF} + 20 \cdot \log\left(\frac{f_C}{f_{REF}}\right) \quad (12)$$

Where PN_{OUT} [dBc/Hz] is the DAC output phase noise, PN_{REF} [dBc/Hz] is the PLL reference clock phase noise, f_C is the DAC output frequency, and f_{REF} is the PLL reference clock frequency

In addition to the reference clock phase noise and jitter, the maximum allowable spur level in the clock spectrum should be limited based on target performance standards such as DOCSIS 3.1.

Additional details on the DAC clock requirements and derivation of the equations noted above are available upon request.

NCO Frequency

The NCO frequency is subject to two types of errors resulting from the NCO and DAC clock frequencies. The first error stems from the NCO itself and is a result of using finite word lengths for calculating the various frequency control factors. As established in the *Quadrature Modulator and NCO* section, the frequency error can be calculated with the following equation:

$$f_{Error} = f_{Desired} - \frac{f_{DAC}}{2^{19} \cdot 2^{33}} \quad (13)$$

This f_{Error} works out to a negligible 1.11µHz when using an f_{DAC} = 5GHz clock rate.

The NCO's fractional registers use 18 bits for the numerator (NFW) and 19 bits for the denominator (DFW). To minimize NCO frequency errors, the DFW can always be programmed to 0x3FFFF while setting the NFW based on the fractional portion of the calculated FCW_{full}. This limits the NCO frequency error to 1.11µHz. Using Matlab code or similar means of calculation can often reduce error to 0Hz.

The second error to the NCO frequency is related to DAC input sampling clock. The NCO synthesizes a frequency based on an exact fraction of the DAC core clock frequency. That fractional value can be calculated using the equation found in the *Quadrature Modulator and NCO* section. Any percentage error in the DAC input clock, either with PLL enabled or disabled, will result in the same percentage error at the NCO output. For example, if the DAC input clock has a tolerance of 10ppm, the NCO output frequency will also have a tolerance of 10ppm.

The DAC PLL does not introduce any frequency error once it is locked. The PLL output frequency is exactly equal to the input reference frequency multiplied by the selected PLL multiplication factor.

Latency

There are two types of latencies in the MAX5857: DAC conversion latency and JESD204B data latency. The DAC latency is given in the Electrical Characteristics table with units of DAC Clock Cycles. The JESD204B Rx LINK layer includes the transmit link latency, the channel latency, and the lane processing latency.

The RLinkRegs.CfgRLinkMFrame.ILADly register will need to be adjusted by the user in the final application environment. This frame clock count for the FIFO read start is dependent on a number of external factors such as FPGA/ASIC transmit delays, overall trace lengths, lane mismatch, and board parasitics. The RxLink latency will have an uncertainty of up to 20 bit clock periods after a reset state. The lane processing delay portion of the JESD204B Rx LINK is 200 SerDes bit clocks.

PRBS Sequence

PRBS7 and PRBS23 are supposed to be inverted according to Table 3 in **http://www.xilinx.com/support/documentation/application_notes/xapp884_PRBS_GeneratorChecker.pdf**

The MAX5857 Rx PHY has an option to invert the data by setting PHY.MISC_REG2.Rx_parallel_data_invert (bit 4). Contact the factory for additional information on using the PRBS pattern checking capabilities of the MAX5857 JESD interface.

DAC Output Impedance Model and Matching Network

A DAC output impedance model is available in an s-parameter file which can be used for the design of an output matching network. When designing the PCB, the following best engineering practices may help:

- OUTP and OUTN trace routes to the matching network should be as short as possible. Similarly, the trace routes from the matching network to any filter should also be as short as possible.
- The OUTP and OUTN traces should be routed symmetrically to reduce any mismatch.
- The environment around OUTP and OUTN pins should be symmetrical. This means that the parasitic environment "seen" by one signal should match environment "seen" by the other signal.
- If OUTP and OUTN cannot use short trace routes, those traces should have matched lengths with mirror symmetry and they should use a 50Ω routed impedance.
- When crossing other signals/supplies routed on other layers, OUTP and OUTN should cross at a 90° angle to these signals/supplies.

- OUTP and OUTN should be routed on an outer board layer and should be kept away from supply decoupling components and traces.
- The AVCLK network should not be placed nor routed in proximity to OUTP and OUTN network.

Thermal Considerations

The use of component-layer, ground plane “pour” is highly recommended for the PCB design. For improved thermal performance, the system design should incorporate direct-contact heatsinking to the device when possible. The thermal resistance values provided in the *Absolute Maximum Ratings* section are based on JEDEC standard 51-12. The application of thermal modeling is highly recommended at the time of system design and a Delphi model is available for system thermal simulations.

Ordering Information

PART NUMBER	TEMP RANGE	PIN-PACKAGE
MAX5857EXE+	-40°C to +85°C	144-FCCSP
MAX5857EXE+T	-40°C to +85°C	144-FCCSP

+Denotes a lead(Pb)-free/RoHS-compliant package.

T = Denotes tape-and-reel.

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	3/18	Initial release	—

For pricing, delivery, and ordering information, please contact Maxim Direct at 1-888-629-4642, or visit Maxim Integrated's website at www.maximintegrated.com.

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